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High-Performance Ternary (4:2) Compressor Based on Capacitive Threshold Logic

Reza Faghih Mirzaee, and Akram Reza

***Abstract*—This paper presents a ternary (4:2) compressor, which is an important component in multiplication. However, the structure differs from the binary counterpart since the ternary model does not require carry signals. The method of capacitive threshold logic (CTL) is used to achieve the output signals directly. Unlike the previously presented similar structure, the entire capacitor network is divided into two parts. This segregation results in higher reliability and robustness against unwanted process, voltage, and temperature (PVT) variations. Simulations are performed by HSPICE and 32nm CNFET technology. Simulation results demonstrate about 94% higher performance in terms of power-delay product (PDP) for the new design over the previous one.**

***Keywords*—(4:2) compressor, ternary logic, multiple-valued logic, CNFET, threshold logic**

I. Introduction

MULTIPLE-VALUED LOGIC (MVL) has attracted significant attention amongst circuit and system designers for the last couple of decades. It uses higher radix based number systems than the traditional binary, where there are only two digits (*'0'* an *'1'*). Number systems with high radices are of particular interest due to fewer required memory cells, interconnections, and pin-outs when it comes to the hardware implementation [1, 2]. On the other hand, a voltage-mode digital electronic system with high radix tends to be noise sensitive, since voltage levels get closer to one another. The most efficient MVL system, which leads to less product cost and complexity than binary, is ternary logic [3].

Multiplication is one of the operations, whose applications are various such as in Digital Signal Processing (DSP) algorithms, microprocessors, and embedded systems [4, 5]. At the first step, multiplicand and multiplier are multiplied. The result is a huge number of partial products, which have to be added in the second step. The addition must be carried out in a parallel manner in order to eliminate carry propagation. Compressors are the computational units for this particular purpose. They perform addition and compression at the same time. A (4:2) compressor is a well-known component in binary logic for the fast accumulation of partial products. It is widely used in multiplication architectures [6, 7].

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This paper deals with partial product reduction in a ternary multiplier. It shows how the structure of a (4:2) compressor differs in ternary and binary logics. The gate-level and transistor-level designs are fully discussed. The method of Capacitive Threshold Logic (CTL) [8] is used in this paper to design a ternary (4:2) compressor. Many complex functions can be implemented with a few numbers of gates and in a short logic depth by this approach [9, 10]. This particular method is the first practically applicable Threshold Logic (TL) technology [10]. The same method has previously been used to design ternary functions as well [11, 12].

Moreover, a ternary (4:2) compressor has been presented in [13] previously (Fig. 1). At first, it uses the same method of CTL to achieve the output carry as well as three scaled Sums. Then, the final value of Sum is selected by a multiplexer, whose selectors come from a ternary decoder. The multiplexer itself is implemented by transmission-gates. Although it does not use many transistors, the implementation method for capacitors has not been mentioned. In addition, the structure is very sensitive to environmental variations. The reason will be given in this paper, and we will show how sensitivity is reduced for our proposed design.

The new design is based on Carbon Nanotube FET (CNFET) technology. It is considered as the most promising alternative to the conventional bulk-CMOS technology, which has faced many serious challenges and difficulties in the nanoscale regime [14]. Both n-type and p-type transistors exist in the CNFET technology. Therefore, the same previous well-known logic styles such as Complementary MOS (CMOS), Pass-Transistor Logic (PTL), Differential Cascode Voltage Switch (DCVS), and Threshold Logic (TL) can be implemented without change and even with higher efficiency. A CNFET-based circuit operates faster and dissipates less power in comparison with its bulk-CMOS counterpart [15, 16]. The ability of adjusting threshold voltage is another unique characteristic, which is in high demand for MVL designs and threshold logic, whose concepts are our main objective in this paper.

The rest of the paper is organized as follows: Section 2 reviews the background knowledge to the topics of this paper. The proposed design is presented in Section 3. Simulation results and comparisons are given in Section 4. Finally, Section 5 concludes the paper.

II. Background Information

This section includes some brief reviews regarding the topics of this paper.

A. (4:2) Compressor in Binary Logic

Although binary logic is not the target of this paper, the (4:2) compressor in binary logic is reviewed quickly for better realization of the ternary model in the next section. Compressors perform addition and compression at the same time. The truth table of the (4:2) compressor is shown in Table I. Unlike its apparent title, the whole block is in fact capable of adding five input variables (Fig. 2a). The reason is that $In_1+In_2+In_3+In_4$ cannot be represented by only two digits (Sum and Carry). Therefore, an extra output signal (C_{out}) is also required to be able to represent the sum of input variables correctly. By involving this additional output, the entire block (Fig. 2a) is now actually capable of adding five input signals (In_1 to In_4 and also C_{in}). Note that C_{out} is as weighed as Carry, otherwise the compressor is called (5:3). As a result, there is no difference which one becomes *'High'* when the sum of input variables is two or three (Table I). In general, an (m:2) compressor requires *m–3* input/output carries [17]. In binary logic, the (4:2) compressor is usually built by using two Full Adders (Fig. 2b).

TABLE I
TRUTH TABLE OF (4:2) COMPRESSOR IN BINARY LOGIC

$In_1+In_2+In_3+In_4+C_{in}$	C_{out} (2^{n+1})	Carry (2^{n+1})	Sum (2^n)
0	0	0	0
1	0	0	1
2	1	0	0
3	1	0	1
4	1	1	0
5	1	1	1

B. Ternary Logic

Ternary logic is the most popular MVL system. Ternary number set can be represented by either balanced or unbalanced ternary digits [2] ($\{-1,0,1\}_3$ or $\{0,1,2\}_3$). The latter notation is actually an extension to the binary numeral system, and it is our objective in this paper. The logic values of '0', '1', and '2' in the unbalanced ternary notation are implemented by 0V, ½V_{DD}, and V_{DD}, respectively. The middle voltage is simply generated by voltage division between the supply rails (ground and power supply). Therefore, there is no need of an additional power supply.

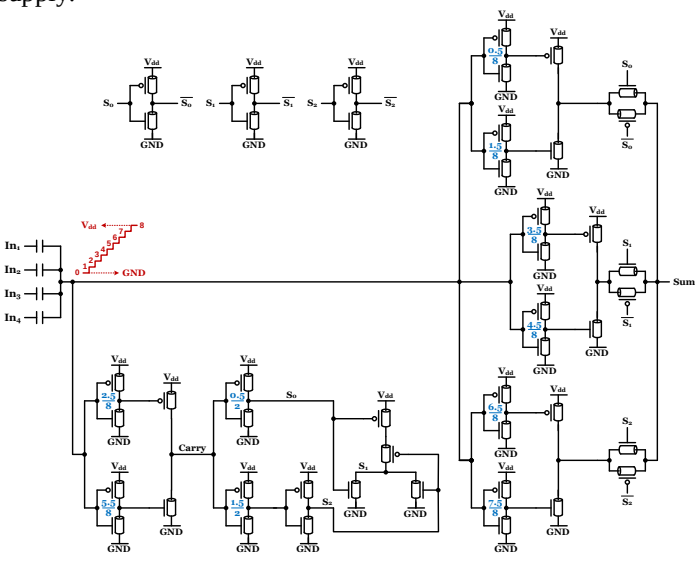

Fig. 1. The previous (4:2) compressor in ternary logic [13].

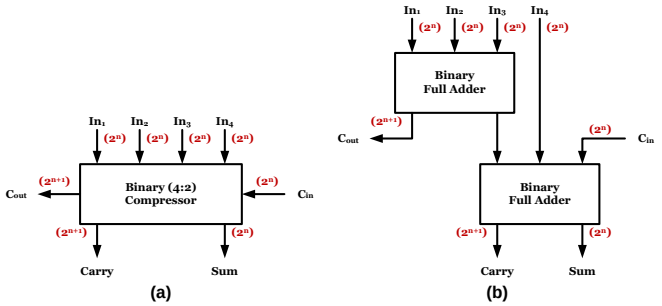

Fig. 2. (4:2) compressor in binary logic, (a) Block, (b) Implementation by two Full Adders.

C. Ternary Logic

Ternary logic is the most popular MVL system. Ternary number set can be represented by either balanced or unbalanced ternary digits [2] ($\{-1,0,1\}_3$ or $\{0,1,2\}_3$). The latter notation is actually an extension to the binary numeral system, and it is our objective in this paper. The logic values of '0', '1', and '2' in the unbalanced ternary notation are implemented by 0V, ½V_{DD}, and V_{DD}, respectively. The middle voltage is simply generated by voltage division between the supply rails (ground and power supply). Therefore, there is no need of an additional power supply.

Ternary functions can be represented in three different ways: 1) Negative (denoted by −), in which the logic value '1' is replaced by '0'; 2) Positive (denoted by +), where the same value is replaced by '2'; and 3) Standard, which takes all possible forms of a ternary digit. The first two definitions are in fact binary functions since they accept only two logic values ('0' and '2'). A method of circuitry (Fig. 3) has been presented in [18] to design ternary adders. This approach is on the basis of the fact that the third definition is the average of the other ones (Eq. 1).

$$STOut = \frac{(Out+)+(Out-)}{2} = \frac{\overline{(\overline{Out}-)}+\overline{(\overline{Out}+)}}{2} \tag{1}$$

In this methodology, two CMOS-like subcircuits, including Pull-Up and Pull-Down Networks (PUN and PDN) take ternary input variables and generate $\overline{Out}+$ and $\overline{Out}-$ (Fig. 3). Then two binary inverters convert them to $Out-$ and $Out+$. Within the final step, two transistors perform voltage division to obtain the standard ternary output (*STOut*).

D. Capacitive Threshold Logic

The arithmetic operation of sum-of-products is initially done by an array of capacitors in CTL. In fact, the capacitor network, consisting of identical capacitors, average the input signals out (Eq. 2).

$$\sum Inputs = \frac{C_{In1}\times V_{In1}+C_{In2}\times V_{In2}+\ldots+C_{InN}\times V_{InN}}{C_{In1}+C_{In2}+\ldots+C_{InN}} = \frac{C(V_{In1}+V_{In2}+\ldots+V_{InN})}{N\times C} = \frac{V_{In1}+V_{In2}+\ldots+V_{InN}}{N} \tag{2}$$

A Boolean function is either linearly separable or not. If so, the output value changes once above a specific threshold, *T* (Eq. 3), and a threshold detector easily discerns it. If not, the output value changes several times (Eq. 4). In this case, there are

several thresholds, from T_1 to T_k, and a Multi-Threshold Threshold Gate (MTTG) is required to generate the proper output [19]. Multi-threshold transistors are an absolute requirement in this method of circuitry to be able to detect different threshold.

$$f = \begin{cases} 0 & \Sigma_{in} < T \\ 1 & \Sigma_{in} > T \end{cases} \tag{3}$$

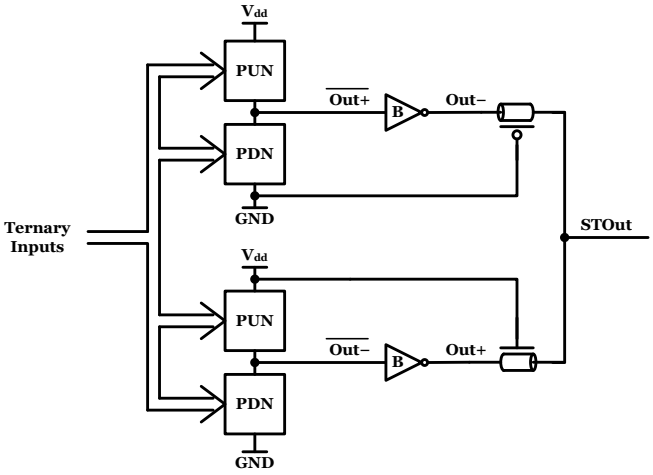

Fig. 3. The method of ternary circuitry presented in [18].

$$f = \begin{cases} 0 & \Sigma_{in} < T_1 \\ 1 & T_1 < \Sigma_{in} < T_2 \\ \cdots & \cdots \\ 0 & T_{k-1} < \Sigma_{in} < T_k \\ 1 & \Sigma_{in} > T_k \end{cases} \tag{4}$$

E. Carbon Nanotube FET

Carbon NanoTube (CNT) is a hollow cylinder created by rolling one or some sheets of graphite. A Multi-Walled CNT (MWCNT) is always metallic, but a Single-Walled CNT (SWCNT) can be metallic or semiconductor depending on its chiral vector, which describes how the carbon atoms are situated along a CNT. Two non-negative integer indices (n_1, n_2) characterize the chiral vector. If $|n_1-n_2|$ is divisible by three, CNT is metallic. Otherwise, it is semiconductor. The semiconducting SWCNTs are used in CNFET as the channel of transistor [20]. Figures 4a and 4b display the side and 3D schematic views of a CNFET, respectively. The distance between the centers of two adjacent CNTs is called *'Pitch'*. The mentioned indices (n_1, n_2) indicate the diameter of a CNT (D_{CNT}) (Eq. 5) [20, 21]. Furthermore, the threshold voltage of a CNFET device can be calculated by Eq. 6 [20, 21].

In the method of CTL, an array of capacitors average the input signals out. Carbon Nanotube Capacitor (CNCAP) [22] can be used for the realization of capacitor in this technology. It is a single CNFET, whose source, drain, and bulk are connected together. As a result, the gate terminal is one of the plates of CNCAP, and the source-drain-bulk junction is the other one.

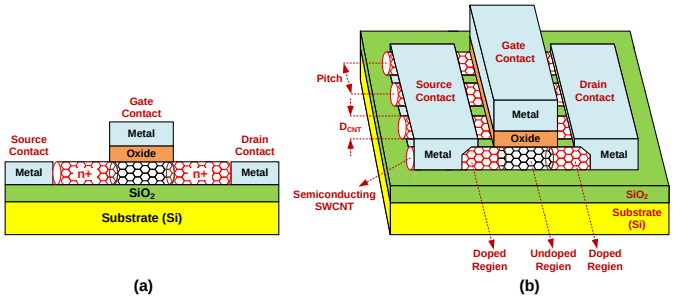

Fig. 4. CNFET device, (a) Side view, (b) 3D schematic view.

$$D_{CNT}\,(nanometer) = 0.0783 \times \sqrt{n_1^{\,2} + n_2^{\,2} + n^1 \times n^2} \tag{5}$$

$$V_{Th} = \frac{0.43}{D_{CNT}\,(nanometer)} \tag{6}$$

III. The Proposed Design

Unlike in binary logic, the two output signals of the (4:2) compressor in ternary logic are capable of representing the sum of input variables for all patterns (Table II). Therefore, there is no need of any extra carry signals (Fig. 5). Another important difference between ternary and binary structures is that the ternary (4:2) compressor cannot be implemented by two FAs. This well-known architecture (Fig. 2b) generates three outputs, which are superfluous in the ternary model. As a result, it loses its usefulness in ternary logic, and the outputs of the ternary (4:2) compressor must be generated by an individual circuit. The method of threshold logic is an appropriate choice for our purpose since it implements logical functions with less complexity, fewer gates, and shorter logic depth [9, 23].

In the method of CTL, an array of capacitors average the input signals out. Then, an MTTG detects different threshold values and accordingly generates the proper output. Although the method of CTL seems attractive, it divides the entire voltage range (from 0V to V_{DD}) into several narrow zones. To be more precise, it will be divided into nine levels (from 0 to 8) if a single capacitor network is used for voltage division among the four ternary inputs. As a result, the entire circuit becomes very sensitive to Process, Voltage, and Temperature (PVT) variations. The same thing happens for the design presented in [13].

Table II.
Truth Table of (4:2) Compressor in Ternary Logic

$In_1+In_2+In_3+In_4$	Carry (3^{n+1})	Sum (3^n)
0	0	0
1	0	1
2	0	2
3	1	0
4	1	1
5	1	2
6	2	0
7	2	1
8	2	2

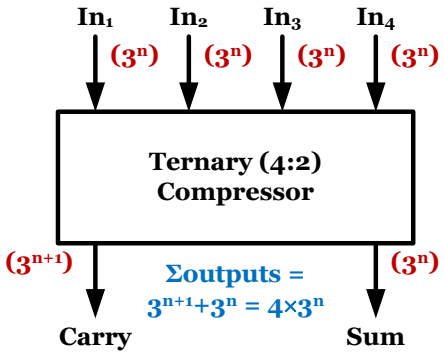

Fig. 5. (4:2) compressor in ternary logic.

TABLE III
TRUTH TABLE OF TERNARY (4:2) COMPRESSOR BASED ON X AND Y (FIG. 6)

$x = In_3+In_4$	$y = In_1+In_2$	Carry	Sum
0	0	0	0
0	1	0	1
0	2	0	2
0	3	1	0
0	4	1	1
1	0	0	1
1	1	0	2
1	2	1	0
1	3	1	1
1	4	1	2
2	0	0	2
2	1	1	0
2	2	1	1
2	3	1	2
2	4	2	0
3	0	1	0
3	1	1	1
3	2	1	2
3	3	2	0
3	4	2	1
4	0	1	1
4	1	1	2
4	2	2	0
4	3	2	1
4	4	2	2

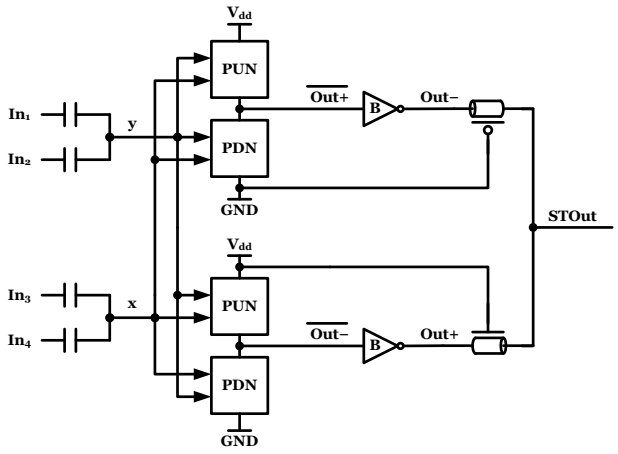

Fig. 6. The proposed model for (4:2) compressor in ternary logic.

In order to increase the level of robustness against unwanted PVT variations, the four input variables are divided into two groups in this paper. Table III displays the truth table based on which the new ternary (4:2) compressor is designed. In this paper, the concept of TL is combined with the approach presented in [18] (Fig. 3). The proposed model is illustrated in Fig. 6. It is treated like there are only two input variables available, x and y ($x, y \in \{0,1,2,3,4\}$).

The values of $\overline{\text{Sum}}+(x,y)$, $\overline{\text{Sum}}-(x,y)$, $\overline{\text{Carry}}+(x,y)$, and $\overline{\text{Carry}}-(x,y)$ are depicted in Table IV. These outputs are either '0' or '2'. A pair of pull-up (PU) and pull-down (PD) networks is required to implement each. Their implementation is based on Eqs. 7 to 14, where the appropriate value(s) of the variables x and y are written by superscript numbers. For example, the term $x^0.y^{3|4}$ (Eq. 14) becomes *'TRUE'* whenever x is '0' and y equals '3' or '4'. Figure 7 shows how the literals such as x^0 and $y^{3|4}$ are generated. Note that the inverted literals are required for the pull-up network, e.g. a p-type transistor must be driven by $\overline{x^0} = x^{1|2|3|4}$ to have the same functionality as an n-type transistor fed by x^0.

TABLE IV
THE VALUES OF $\overline{\text{Sum}}+$, $\overline{\text{Sum}}-$, $\overline{\text{Carry}}+$, AND $\overline{\text{Carry}}-$ FOR THE (4:2) COMPRESSOR IN TERNARY LOGIC

x	y	$\overline{\text{Carry}}+$	$\overline{\text{Carry}}-$	$\overline{\text{Sum}}+$	$\overline{\text{Sum}}-$
0	0	2	2	2	2
0	1	2	2	2	0
0	2	2	2	0	0
0	3	2	0	2	2
0	4	2	0	2	0
1	0	2	2	2	0
1	1	2	2	0	0
1	2	2	0	2	2
1	3	2	0	2	0
1	4	2	0	0	0
2	0	2	2	0	0
2	1	2	0	2	2
2	2	2	0	2	0
2	3	2	0	0	0
2	4	0	0	2	2
3	0	2	0	2	2
3	1	2	0	2	0
3	2	2	0	0	0
3	3	0	0	2	2
3	4	0	0	2	0
4	0	2	0	2	0
4	1	2	0	0	0
4	2	0	0	2	2
4	3	0	0	2	0
4	4	0	0	0	0

The proposed design is depicted in Figs. 7, 8, and 9, where each transistor is marked by a number whose value indicates D_{CNT}. There are three CNTs under the gate of all transistors except the ones implement capacitors (Fig. 7). These transistors have 300 CNTs. In order to achiece even more capacitance, channel, and doped CNT source- and drain-side extension regions for these transistors are lengthened by 130nm. Figure 10 shows the transient response of the proposed ternary (4:2) compressor.

$$\overline{Sum}+(PU)=(x^0+x^3)(y^{0|1}+y^{3|4})+(x^1+x^4)(y^0+y^2+y^3)+x^2(y^1+y^2+y^4) \quad (7)$$

$$\overline{Sum}+(PD)=(x^0+x^3)y^2+(x^1+x^4)(y^1+y^4)+x^2(y^0+y^3) \quad (8)$$

$$\overline{Sum}-(PU)=(x^0+x^3)(y^0+y^3)+(x^1+x^4)y^2+x^2(y^1+y^4) \quad (9)$$

$$\overline{Sum}-(PD)=(x^0+x^3)(y^1+y^2+y^4)+(x^1+x^4)(y^{0|1}+y^{3|4})+x^2(y^0+y^2+y^3) \quad (10)$$

$$\overline{Carry}+(PU)=x^{0|1}+x^2y^{0|1|2|3}+x^3y^{0|1|2}+x^4y^{0|1} \quad (11)$$

$$\overline{Carry}+(PD)=x^2y^4+x^3(y^3+y^4)+x^4(y^2+y^3+y^4) \quad (12)$$

$$\overline{Carry}-(PU)=x^0y^{0|1|2}+x^1y^{0|1}+x^2y^0 \quad (13)$$

$$\overline{Carry}-(PD)=x^0y^{3|4}+x^1y^{2|3|4}+x^2y^{1|2|3|4}+x^{3|4} \quad (14)$$

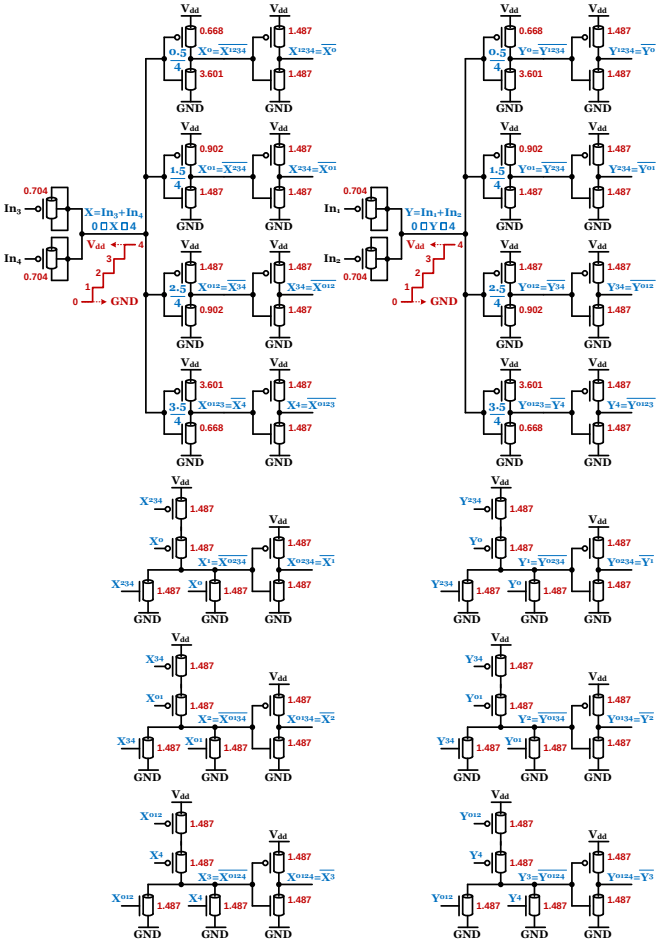

Fig. 7. Transistor-level implementation of the required literals based on x and y.

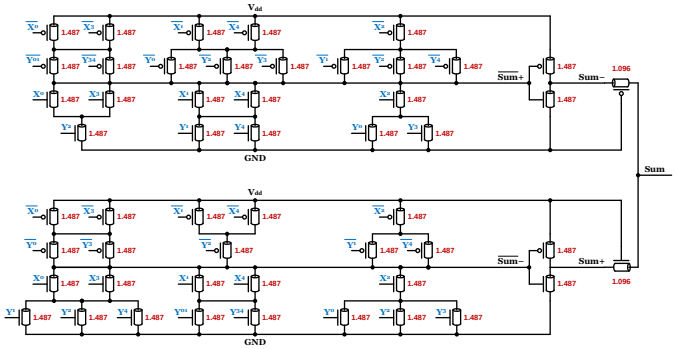

Fig. 8. The proposed circuit (Sum generator).

IV. Simulation Results and Comparisons

The proposed and previous designs are simulated by HSPICE and the Compact SPICE model for 32nm CNFET-based circuits [20, 24], including all non-idealities. This standard model has been designed for unipolar, MOSFET-like CNFET devices, where each transistor has one or more CNTs. The implementation method for capacitors has not been mentioned in [13], and hence ideal capacitors are considered for simulation purpose. The new design uses CNCAPs, which are totally compatible with the CNFET technology.

Simulations are performed in three different power supply voltages (1V, 0.9V, and 0.8V) at room temperature. The input pattern plotted in Fig. 10 with the operating frequency of 1GHz is fed to the circuits. The output load of 1 femto Farad capacitor is applied for each output node (Sum and Carry). Maximum delay among the 81 transitions and the average power consumption during these transitions are reported in Table V. Their multiplication is known as Power-Delay Product (PDP), which makes a balance between these two evaluating parameters (Eq. 15).

Simulation results demonstrate the superiority of the new design over the one presented in [13]. For example, the proposed (4:2) compressor operates almost twice faster and cosumes about 27μW less power than the previous version. In overall, efficiency increases about 94% in terms of PDP. One of the drawbacks of the previous design is that the output Sum is generated from the output carry. Not only does the critical path of the cell increase, but also any loads on the output carry node also affects the output Sum. This is the reason why it operates slowly. In the proposed design, both outputs are generated consurrently, and they do not affect each other adversely.

TABLE V
SIMULATION RESULTS

Design	Delay ($\times10^{-12}$s)	Power ($\times10^{-6}$W)	PDP ($\times10^{-16}$J)
V_{DD} = 1V			
Proposed	67.054	7.0909	4.7548
Previous	82.548	40.613	33.525
V_{DD} = 0.9V			
Proposed	80.763	3.4651	2.7985
Previous	158.74	30.653	48.660
V_{DD} = 0.8V			
Proposed	275.76	1.8831	5.1927
Previous	Failed	Failed	Failed

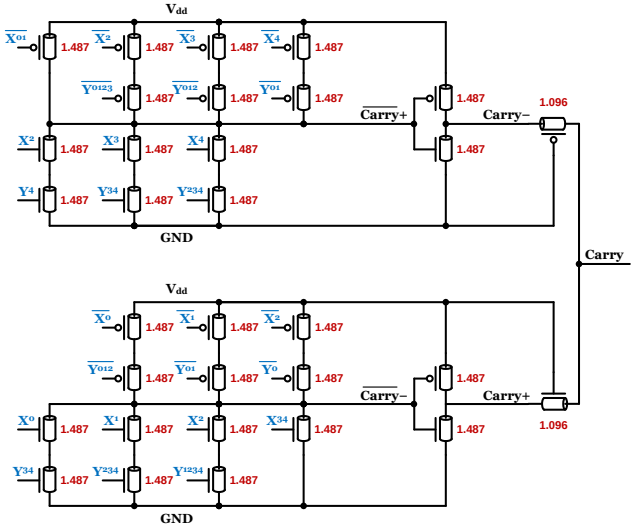

Fig. 9. The proposed circuit (Carry generator).

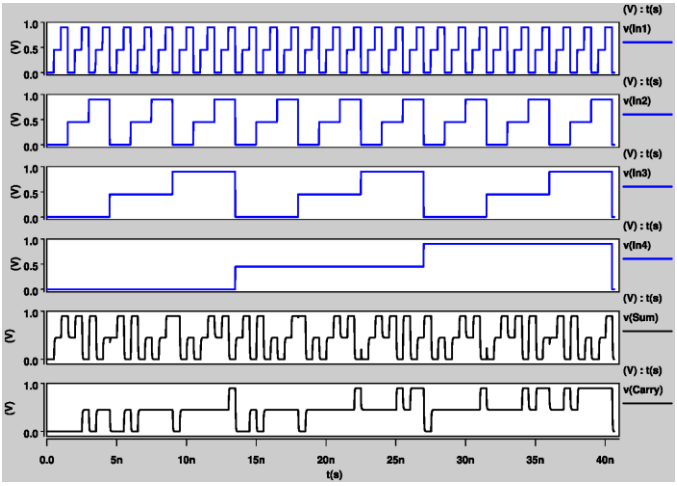

Fig. 10. Transient response for the proposed ternary (4:2) compressor.

$$PDP = Max(Delay) \times Avg(Power) \qquad (15)$$

The reason for high power consumption of the previous design is because of the scaled inverters (Fig. 1). An ordinary CMOS inverter does not dissipate static power due to the fact that either the n-type or p-type transistor is completely switched off. However, the scaled inverters are not fed by a full-swing signal. Therefore, neither of the transistors are entirely off. As a result, static current flows from V_{DD} to the ground inside every scaled inverter. Although there are some scaled inverters in the proposed design as well, they do not dissipate as much power as the ones in the previous design do. The reason is that the integrated capacitor network of the previous design divides the entire voltage range into nine different levels (from 0 to 8). The scaled inverters do not dissipate static power in case the sum of input variables are either 0 or 8. Otherwise, they do consume static power. Therefore, the probability of static power dissipation in the scaled inverters is $\frac{7}{9}$.

The input variables are divided into two groups in the proposed design. There are two segregated capacitor netwroks. Each one divides the voltage range into five levels. Static current flows in three of them. Therefore, there are static power dissipation with the probability of $\frac{3}{5}$ in either of the networks. The total probability is $\frac{3}{5}\times\frac{3}{5}=\frac{9}{25}$ due to the fact that the two networks operate independently. Thus, the previous design has statistically more tendency to consume static power. Moreover, there are eight scaled inverters in our proposed (4:2) compressor (Fig. 7), whereas there are 10 ones in the previous design (Fig. 1). Therefore, there are more components which are prone to dissipate power.

In order to compare static power more precisely, it is measured for 81 different input patterns while the input signals are kept unchanged. The average amount is reported in Table VI. The proposed design consumes approximately 29μW less static power.

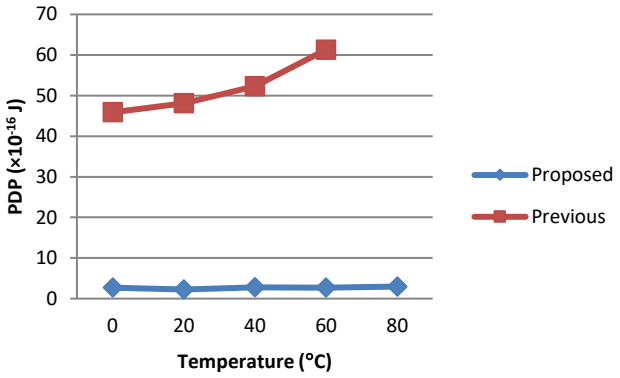

Fig. 11. PDP versus temperature.

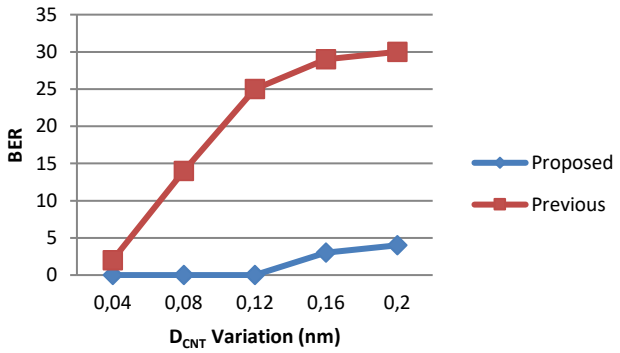

Fig. 12. BER per 30 runs for different D_{CNT} variations each.

TABLE VI
COMPARISON OF TERNARY (4:2) COMPRESSORS ATTRIBUTES

Design	#Voltage Levels	Narrowest Voltage Range (V)	Capacitor Implementation Method	Average Static Power (μW)
Proposed	5	$\frac{V_{DD}}{4}$	CNCAP	1.6299
Previous	9	$\frac{V_{DD}}{8}$	Not mentioned (Considered Ideal)	31.072

As the number of voltage levels increases in the TL-based circuits, they become more and more sensitive to PVT variations. Table VI shows the number of voltage levels and the narrowest voltage range for both designs. The new structure has wider voltage range, and consequently less sensitivity to the unwanted environmental variations. As it is shown in Table V, the previous design fails to operate correctly in 0.8V power supply. It also stops working properly in 80°C. PDP variations versus different ambient temperatures are plotted in Fig. 11.

Furthermore, the proper operation of both designs is put under investigation in the presence of process variation. Monte Carlo transient analysis [25] with 30 iterations is considered to study how sensitive the designs are against the variation of D_{CNT}, which has the most significant impact on the performance of the CNFET-based circuits. Distribution of the diameter is assumed as Gaussian [26]. The expected variability for each mean diameter value is from 0.04nm to 0.2nm [27]. Bit Error Rate (BER) per 30 Monte Carlo runs for different D_{CNT} variations is plotted in Fig. 12. Taking experiment shows that the segregation of the capacitor network improves the reliability and robustness of the proposed design against process variation considerably in comparison with the design presented in [13].

V. Conclusion

The current work presents a novel ternary (4:2) compressor based on capacitive threshold logic. Although this method results in fewer transistors in comparison with other logic styles, it might lead to high sensitivity to undesirable PVT variations if the initial voltage division results in several close voltage levels. Investigations in this work illustrate that smaller capacitor networks result in circuits with higher tolerance against PVT variations. The proposed ternary (4:2) compressor makes an excellent trade-off between simplicity and robustness. While the previous design fails to operate correctly in 0.8V or 80°C, the new design eliminates these drawbacks by dividing the entire capacitor network into two. In addition, sensitivity to process variation has been decreased considerably.

References

[1] G. Jaberipur and M. Ghodsi, "High radix signed digit number systems: representation paradigms", *Scientia Iranica*, vol. 10, no. 4, pp. 383-391, 2003.

[2] E. Dubrova, "Multiple-valued logic in VLSI: challenges and opportunities", *Proceedings of NORCHIP'99*, pp. 340-350, 1999.

[3] S.L. Hurst, "Multiple-valued logic, its status and its future", *IEEE Transactions on Computers*, vol. C-33, no. 12, pp. 1160-1179, 1984, **DOI:** 10.1109/TC.1984.1676392.

[4] S.K. Hsu, S.K. Mathew, M.A. Anders, B.R. Zeydel, V.G. Oklobdzija, R.K. Krishnamurthy, and S.Y. Borkar, "A 110 GOPS/W 16-bit multiplier and reconfigurable PLA loop in 90-nm CMOS", *IEEE Journal of Solid-State Circuits*, vol. 41, no. 1, pp. 256-264, 2006, **DOI:** 10.1109/JSSC.2005.859893.

[5] M.E. Kaihara and N. Takagi, (2008). "Bipartite modular multiplication method", *IEEE Transactions on Computers*, vol. 57, no. 2, pp. 157-164, 2008, **DOI:** 10.1109/TC.2007.70793.

[6] J. Gu, and C.-H. Chang, "Ultra low voltage, low power 4-2 compressor for high speed multiplications", *Proceedings of the International Symposium on Circuits and Systems*, 5, pp. 321-324, 2003, **DOI:** 10.1109/ISCAS.2003.1206267.

[7] A. Pishvaie, G. Jaberipur, and A. Jahanian, "Improved CMOS (4; 2) compressor designs for parallel multipliers", *Computers and Electrical Engineering*, vol. 38, no. 6, pp. 1703-1716, 2012, **DOI:** 10.1016/j.compeleceng.2012.07.015.

[8] H. Ozdemir, A. KepKep, B. Pamir, Y. Leblebici, and U. Cilingiroglu, "A capacitive threshold-logic gate", *IEEE Journal of Solid-State Circuits*, vol. 31, no. 8, pp. 1141-1150, 1996, **DOI:** 10.1109/4.508261.

[9] V. Beiu, J.M. Quintana, and M.J. Avedillo, "VLSI implementations of threshold logic-a comprehensive survey", *IEEE Transactions on Neural Networks*, vol. 14, no. 5, pp. 1217-1243, 2003, **DOI:** 10.1109/TNN.2003.816365.

[10] A. Stokman, "Implementation of threshold logic", *M.Sc. Thesis, Delft University of Technology*, 1998.

[11] R. Faghih Mirzaee, M.H. Moaiyeri, M. Maleknejad, K. Navi, and O. Hashemipour, "Dramatically low-transistor-count high-speed ternary adders", *IEEE 43rd International Symposium on Multiple-Valued Logic*, pp. 170-175, 2013, **DOI:** 10.1109/ISMVL.2013.24.

[12] R. Faghih Mirzaee and K. Navi, "Optimized adder cells for ternary ripple-carry addition", *IEICE Transactions on Information and systems*, vol. E97-D, no. 9, pp. 2312-2319, 2014, **DOI:** 10.1587/transinf.2013LOP0007.

[13] S. Tabrizchi, H. Sharifi, F. Sharifi, and K. Navi, "A novel design approach for ternary compressor cells based on CNTFETs", *Circuits, Systems, and Signal Processing*, vol. 35, no. 9, pp. 3310-3322, 2016, **DOI:** 10.1007/s00034-015-0197-z.

[14] A. Raychowdhury and K. Roy, "Carbon nanotube electronics: design of high-performance and low-power digital circuits", *IEEE Transactions on Circuits and Systems I*, vol. 54, no. 11, pp. 2391-2401, 2007, **DOI:** 10.1109/TCSI.2007.907799.

[15] J. Appenzeller, "Carbon nanotube for high-performance electronics-progress and prospect", *Proceedings of IEEE*, vol. 96, no. 2, pp. 201-211, 2008, **DOI:** 10.1109/JPROC.2007.911051.

[16] A. Rahman, I. Guo, S. Datta, and M.S. Lundstrom, "Theory of ballistic nanotransistors", *IEEE Transactions on Electron Devices*, vol. 50, no. 9, pp. 1853-1864, 2003, **DOI:** 10.1109/TED.2003.815366.

[17] S. Mehrabi, R. Faghih Mirzaee, S. Zamanzadeh, and A. Jamalian, "A new 16-bit×16-bit multiplier architecture by m:2 and m:3 compressors", *International Journal of Information and Electronics Engineering*, vol. 6, no. 2, pp. 79-83, 2016, **DOI:** 10.18178/IJIEE.2016.6.2.599.

[18] R. Faghih Mirzaee, K. Navi, and N. Bagherzadeh, "High-efficient circuits for ternary addition", *VLSI Design*, vol. 2014, article ID 534587, pp. 1-15, 2014, **DOI:** 10.1155/2014/534587.

[19] D.R. Haring, "Multi-threshold threshold elements", *IEEE Transactions on Electronic Computers*, vol. EC-15, no. 1, pp. 45-65, 1966, **DOI:** 10.1109/PGEC.1966.264375.

[20] J. Deng, "Device modeling and circuit performance evaluation for nanoscale devices: Silicon technology beyond 45 nm node and carbon nanotube field effect transistors", *Ph.D. Thesis, Stanford University*, 2007.

[21] N. Maleknejad, R. Faghih Mirzaee, K. Navi, and A. Dargahi, "A systematic approach to design Boolean functions using CNFETs and an array of CNFET capacitors", *Journal of Circuits, Systems, and Computers*, vol. 23, no. 3, pp. 1-35, 2014, **DOI:** 10.1142/S0218126614500352.

[22] Y.B. Kim and Y.-B. Kim, "High speed and low-power transceiver design with CNFET and CNT bundle interconnect", *IEEE International SOC Conference*, pp. 152-157, 2010, **DOI:** 10.1109/SOCC.2010.5784733.

[23] J.L. Garcia, J.F. Ramos, and A.G. Bohorquez, "A balanced capacitive threshold logic gate", *Analog Integrated Circuits and Signal Processing*, vol. 40, no. 1, pp. 61-69, 2004, **DOI:** 10.1023/B:ALOG.0000031434.48142.a3.

[24] Stanford University CNFET Model website, 2008, Available at: https://nano.stanford.edu/model.php.

[25] S. Director, and G. Hachtel, "The simplicial approximation approach to design centering", *IEEE Transactions on Circuits and Systems*, vol. 24, no. 7, pp. 363-372, 1977, **DOI:** 10.1109/TCS.1977.1084353.

[26] K. El Shabrawy, K. Maharatna, D. Bagnall, and B.M. Al-Hashimi, "Modeling SWCNT bandgap and effective mass variation using a Monte Carlo approach", *IEEE Transactions on Nanotechnology*, vol. 9, no. 2, pp. 184-193, 2010, **DOI:** 10.1109/TNANO.2009.2028343.

[27] H. Shahidipour, A. Ahmadi, and K. Maharatna, "Effect of variability in SWCNT-based logic gates", *Proceedings of 12th International Symposium on Integrated Circuits*, pp. 252-255, 2009.