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Study of an open-switch fault detection algorithm for a three-phase interleaved DC–DC boost converter in a photovoltaic system

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Abstract: This paper presents a novel fault detection algorithm for a three-phase interleaved DC–DC boost converter integrated in a photovoltaic system. Interleaved DC–DC converters have been used widely due to their advantages in terms of efficiency, ripple reductions, modularity and small filter components. The fault detection algorithm depends on the input current waveform as a fault indicator and does not require any additional sensors in the system. To guarantee service continuity, a fault tolerant topology is achieved by connecting a redundant switch to the interleaved converter. The proposed fault detection algorithm is validated under different scenarios by the obtained results.

Key words: DC–DC converters, fault diagnosis, interleaved boost converter, open switch fault, photovoltaic (PV) system

1. Introduction

The energy demand is consistently increasing throughout the globe year after year. Currently, the electric power industry is highly dependent on the use of fossil fuels which has adverse consequences like continuous climatic changes. With the continuous decrease in supplies of such fossil fuels and the increase in its prices, the use of alternative energy sources is becoming more than necessary. Therefore, the entire world is turning towards generation of electricity using renewal energy sources. Among them, photovoltaic power is gaining more attention in various electrical applications, as sunshine required to produce electricity is available all year long and everywhere in the world [1, 2].

A photovoltaic power supply system typically produces high currents and low voltage levels that must be managed by a power converter. Hence, a DC–DC boost converter is required to supply the maximum power produced by the photovoltaic generator to the load at any climatic conditions [3–7]. However, the classical DC-DC boost converter will be unable to handle high input current if the input voltage is low. The high input current levels can lead to increased current stress and semiconductor devices losses in the converter. To solve these issues, the interleaved boost converter is suggested in literature [8–12].

The interleaved DC–DC boost converter (IBC) is composed of n phases, whose currents are phase shifted by $2\pi/n$ radians. Interleaving techniques provide good solution to reduce the input current stress due to the input current being distributed equally among the n phases of the IBC. Such operation provides great advantages such as high efficiency, ripple reductions, modularity and small filter components [8–10].

The reliability and efficiency of the interleaved DC–DC boost converter can be compromised by common failures. Electrolytic capacitors and power switches are the components that are most likely to fail due to the high mechanical and thermal stresses they endure inside the IBC [13, 14]. The major reason power switches fail, which can result in open-circuit and short-circuit problems, is an excess of electrical and thermal stresses [15]. Most power switch drives currently have a short-circuit fault protection as a common practice [16].

Unlike other DC–DC converter topologies, the IBC will continue to operate even if a power switch for one phase fails. Despite the fact that this demonstrates the great reliability of the converter, but still it will suffer from excessive output current ripple. Therefore, a real-time fault tolerant strategy is required to prevent current ripple from exceeding acceptable limits and guarantee service continuity.

In the literature, several publications have appeared documenting fault diagnosis methods for power converters [17–25]. The magnetic component (inductor or transformer) voltage is measured by an auxiliary winding in the magnetic core and used for fault diagnosis for DC–DC converters in [17]. In [18], the inductor current form is used as fault indicator for the boost converter. A fault diagnosis of a T-type three-level inverter based on a finite-state machine tracking state transitions and rough set theory is presented in [19]. In [20], a fault diagnostic method for the interleaved DC–DC boost converter based on the dc-link current derivative sign is proposed. Reference [21] proposed an open and short circuit switch fault diagnosis method for non-isolated DC–DC converters. In [22], a novel fault-tolerant topology for an H-bridge DC–DC converter is proposed. In [23], a fault diagnosis based on the DC–link current pulse forms of a ZVS converter is proposed. A fault detection method for a three-level DC–DC converter by monitoring the flying capacitor voltage is proposed in [24]. In [25], a fault-tolerant control under an open-circuit fault was proposed for three-level NPC converters.

The fault detection methods published in [18] and [21] are capable of detecting open-switch faults in interleaved DC–DC converters, but they require one current sensor per phase (three total for a three-phase IBC), which is not cost-effective. To avoid increasing costs and complexity, the inputs of the diagnostic methods should be limited to the control variables.

This paper presents a new and an alternative open-switch fault detection algorithm for three-phase interleaved DC–DC converters. This algorithm is based on the input current waveform and hence does not require additional sensors in the system. In Section 2, an overview of the system configuration is presented. Three-phase interleaved DC–DC boost converter analysis is

presented in Section 3, after which the proposed open-switch switch fault detection algorithm and fault tolerant control are described. Section 4 presents and discusses the results obtained to validate the proposed fault detection algorithm and fault-tolerant control for the PV system when an open-switch fault occurs in the interleaved DC–DC converter. Finally, in Section 5, the conclusion is reported.

2. Systems configuration

Figure 1 shows the complete block diagram structure of the proposed system. The PV array is connected to the load through a 3-phase interleaved DC–DC boost converter. The amount of power produced by the PV array relies on a variety of parameters and climatic conditions, including temperature, solar irradiance, shaded condition, load voltage, and others. Therefore, the converter is controlled using the MPPT control technique in order to extract the most power out of the PV array. The Perturb and Observe (P&O) control algorithm is the most commonly used MPPT technique because of its reliability and simplicity [3–7, 18]. Hence, it is implemented in this paper. The P&O algorithm we applied is detailed in [18].

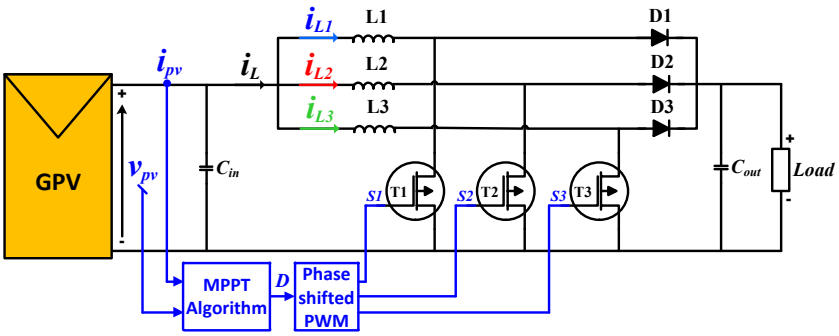


Fig. 1. Electrical circuit of the three-phases interleaved DC–DC boost converter PV system

The three-phase interleaved DC–DC boost converter circuit is formed by three independent boost switching units, which are named phases or legs. Essentially, each of the three units will operate in the same way as the classical boost converter. Thus, the IBC circuit consists of three similar boost inductors ($L1$, $L2$, and $L3$), three power switches ($T1$, $T2$ and $T3$), and three power diodes ($D1$, $D2$, and $D3$). The IBC phases are linked with an output capacitor filter C_{out}, and a load. In this configuration, the duty ratio D generated by the MPPT technique is the same for all phases, but each phase is phase shifted by $2\pi/3$ radians (120°). Moreover, the high input current is divided and shared across all paralleled inductors, where the average of the inductor currents (i_{l1}, i_{l2} and i_{l3}) are evenly distributed with a phase shift of 120°, thus consequently the input current and output voltage ripple will be reduced.

Figure 2 shows the variation of the input current ripple according to the duty ratio for different numbers of phases. Observably, the ripple of the input current is reduced proportionally as the number of phases increases [8, 9, 11].

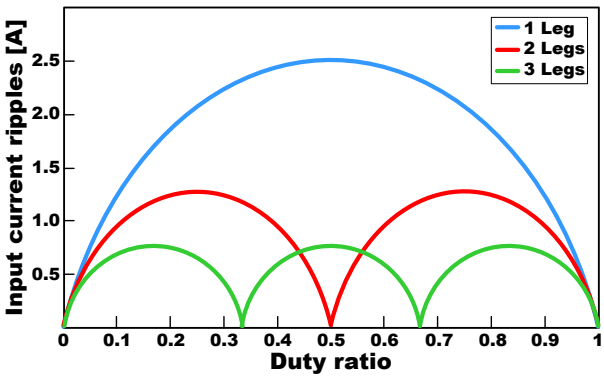


Fig. 2. Input current ripple variations according to the duty ratio

Table 1 lists the PV array parameters. The PV array consists of four BP-365-TS photovoltaic modules and can produce a maximum output of 260 W at 1 000 W/m^2 solar irradiation.

Table 1. PV array parameters

Parameter name	Symbol	Value	Unit
Number of module in parallel	N_p	2	
Number of module in series	N_s	2	
Maximum power	$P_{\max}$	260	W
Voltage at $P_{\max}$	V_{mp}	17.4	V
Current at $P_{\max}$	I_{mp}	15	A

Table 2 lists the three-phase interleaved DC–DC boost converter parameters. The input inductors and output capacitor values were obtained using analytical methods described in [9].

Table 2. Parameters of the three-phase interleaved DC–DC boost converter

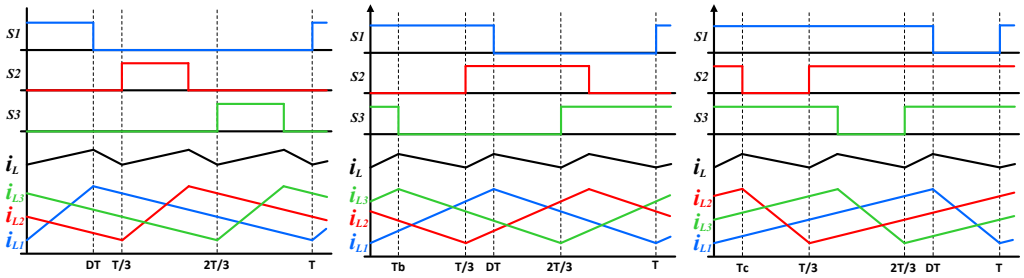
Parameter name	Symbol	Value	Unit
Load resistance	R	12	Ω
Inductances	L	1	mH
Output capacitance	C_{out}	100	µF
Input capacitance	C_{in}	10	µF
Switching frequency	f_s	5	kHz

3. Fault diagnostic method

3.1. Three-phase interleaved DC–DC boost converter analysis

Figure 3 illustrates the basic operation of the three-phase interleaved DC–DC boost converter in continuous conduction mode (CCM) for three cases according to the duty ratio value [8,9].

1. **Case A:** The converter can be in this case when the duty ratio is lower than $\frac{1}{3}$ $\left(D < \frac{1}{3}\right)$. As shown in Fig. 3(a), during the interval $[0, DT]$ only one switch ($T1$) is turned on, thus forcing the inductor current i_{L1} to increase and, consequently, increasing the input current i_L. As all the switches are turned off during the interval $[DT, T/3]$, the inductor currents and the input current decrease.
2. **Case B:** The converter can be in this case when the duty ratio is between $\frac{1}{3}$ and $\frac{2}{3}$ $\left(\frac{1}{3} < D < \frac{2}{3}\right)$. As shown in Fig. 3(b), during the interval $[0, T_b]$ two switches ($T1$ and $T3$) are turned on, forcing the inductor currents i_{L1} and i_{L3} to increase and, as a result, increasing the input current i_L. During the interval $[T_b, T/3]$, as the switch $T3$ turns off, the inductor currents i_{L3} decrease, causing the input current i_L to decrease, but, the inductor current i_{L1} continues to increase and the inductor current i_{L2} continues to decrease.
3. **Case C:** The converter can be in this case when the duty ratio is between $\frac{2}{3}$ and 1 $\left(D > \frac{2}{3}\right)$. As shown in Fig. 3(c), during the interval $[0, T_c]$ all switches are turned on, forcing the inductor currents i_{L1}, i_{L2} and i_{L3} to increase and, consequently, increasing the input current i_L. During the interval $[T_c, T/3]$, as the switch $T2$ turns off, the inductor currents i_{L2} decrease, causing the input current i_L to decrease, however, the current i_{L1} and i_{L3} continue to increase.



(a) Currents and gate signals in the case: $0 < DT < T/3$

(b) Currents and gate signals in the case: $T/3 < DT < 2T/3$

(c) Currents and gate signals in the case: $2T/3 < DT < T$

Fig. 3. Different cases of the three-phase interleaved DC–DC boost converter

The previous analysis is applied to all different intervals of each case according to switching patterns of each subinterval. Table 3 summarizes the switching pattern, duty ratio and input current slope sign for each subinterval. Where $\overline{S1}$, $\overline{S2}$, and $\overline{S3}$ are $S1$, $S2$ and $S3$ compliments, respectively.

Table 3 can be simplified using a truth table and transformed into a pseudocode to estimates the input current slope sign S^*_{iL} based on the duty ratio and switching pattern, as shown in Fig. 4:

Table 3. Sign analysis of the input current

Duty ratio	Switching pattern	Input current slope sign
$0 < D < \frac{1}{3}$	$S1 \quad \overline{S2} \quad \overline{S3}$	*Positive*
	$\overline{S1} \quad S2 \quad \overline{S3}$	
	$\overline{S1} \quad \overline{S2} \quad S3$	
	$\overline{S1} \quad \overline{S2} \quad \overline{S3}$	*Negative*
$\frac{1}{3} < D < \frac{2}{3}$	$S1 \quad \overline{S2} \quad S3$	*Positive*
	$S1 \quad S2 \quad \overline{S3}$	
	$\overline{S1} \quad S2 \quad S3$	
	$S1 \quad \overline{S2} \quad \overline{S3}$	*Negative*
	$\overline{S1} \quad S2 \quad \overline{S3}$	
	$\overline{S1} \quad \overline{S2} \quad S3$	
$\frac{2}{3} < D < 1$	$S1 \quad S2 \quad S3$	*Positive*
	$S1 \quad \overline{S2} \quad S3$	*Negative*
	$S1 \quad S2 \quad \overline{S3}$	
	$\overline{S1} \quad S2 \quad S3$	

if $(D > 0$ **AND** $D \leq 1/3)$ ***then***
  spv $\leftarrow S1$ **OR** $S2$ **OR** $S3$
else if $(D > 2/3$ **AND** $D \leq 2/3)$ ***then***
  spv $\leftarrow (S1$ **AND** $S2)$ **OR** $(S1$ **AND** $S3)$ **OR** $(S2$ **AND** $S3)$
else if $(D > 2/3$ **AND** $D \leq 1)$ ***then***
  spv $\leftarrow S1$ **AND** $S2$ **AND** $S3$
end if
if (spv) ***then***
  $S^*_{iL} \leftarrow$ Positive
else
  $S^*_{iL} \leftarrow$ Negative
end if

Fig. 4. Pseudocode for estimating the input current slope sign

3.2. Open-circuit switch fault detection algorithm

The fault detection method published in [18] is capable of detecting open-switch faults in interleaved DC−DC converters, but it requires three current sensors for a three-phase IBC, which is not cost-effective. To avoid increasing costs and complexity, the proposed fault detection algorithm depends on the input current waveform as a fault indicator and does not require any additional sensors in the system.

As seen in Fig. 5, when a fault occurs in switch $T2$ (at time T_F) the inductor current i_{L2} continues to decrease until it reaches zero even while $S2$ is ON. This will have an impact on the input current i_L and cause it to decrease when it should be increasing.

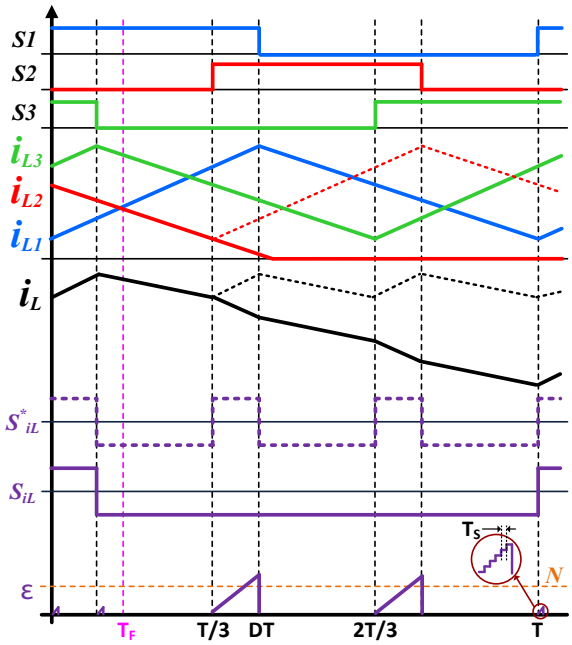


Fig. 5. Currents and gate signals after an open-switch fault occurrence in $T2$

The proposed fault detection algorithm uses the pseudocode shown in Fig. 4 to estimate the input current slope sign S^*_{iL} and compares it with the actual measured input current slope sign S_{iL}. If the two signals S^*_{iL} and S_{iL} differ, the algorithm determines whether a fault has occurred. The actual measured input current slope sign S_{iL} will be delayed in comparison to the estimated input current slope sign S^*_{iL} due to the power switches, sensors delays, and dead times, therefore a counter signal "ε" is introduced to avoid false fault detections.

The counting time N must be greater than the total delay time T_d:

$$N \cdot T_s > T_d \,, \tag{1}$$

where T_s is the sampling period.

Nevertheless, even while the analysis of S^*_{iL} and S_{iL} signals difference can detect faulty operations, it is insufficient to identify and locate the faulty switch $T2$. To locate the faulty switch, the whole switching period T must be analyzed and the error counter signal ε is divided into three intervals (number of phases) for each switching period:

– ε_1: The error counter signal for the first interval is under $\frac{1}{3}T$;

– ε_2: The error counter signal for the second interval is between $\frac{1}{3}T$ and $\frac{2}{3}T$;

– ε_3: The error counter signal for the third interval is between $\frac{2}{3}T$ and T.

For example, the previous open-switch fault in $T2$ can be identified and located when the duty ratio is between $\frac{1}{3}$ and $\frac{2}{3}$, and the error counter signal is greater than the counting time N for both the second and third intervals ($\varepsilon_2 \geq N$ and $\varepsilon_3 \geq N$).

Table 4 lists the criteria for each power switch failure based on the duty ratio and error counter signals.

Table 4. Fault identification and localization criteria based on duty ratio and error signals

Duty ratio	Error signal criteria	Faulty switch
$0 < D < \frac{1}{3}$	$\varepsilon_1 \geq N$	$T1$
	$\varepsilon_2 \geq N$	$T2$
	$\varepsilon_3 \geq N$	$T3$
$\frac{1}{3} < D < \frac{2}{3}$	$\varepsilon_1 \geq N$ **AND** $\varepsilon_2 \geq N$	$T1$
	$\varepsilon_2 \geq N$ **AND** $\varepsilon_3 \geq N$	$T2$
	$\varepsilon_3 \geq N$ **AND** $\varepsilon_1 \geq N$	$T3$
$\frac{2}{3} < D < 1$	$\varepsilon_3 \geq N$	$T1$
	$\varepsilon_1 \geq N$	$T2$
	$\varepsilon_2 \geq N$	$T3$

Figure 6 shows the fault identification and localization pseudocode, where $F1$, $F2$, and $F3$ are the fault diagnostic variables for an open-switch fault in $T1$, $T2$, or $T3$, respectively:

if $(D > 0$ **AND** $D \leq 1/3)$ ***then***
  $F1 \leftarrow \varepsilon_1 \geq N$
  $F2 \leftarrow \varepsilon_2 \geq N$
  $F3 \leftarrow \varepsilon_3 \geq N$
else if $(D > 2/3$ **AND** $D \leq 2/3)$ ***then***
  $F1 \leftarrow \varepsilon_1 \geq N$ **AND** $\varepsilon_2 \geq N$
  $F2 \leftarrow \varepsilon_2 \geq N$ **AND** $\varepsilon_3 \geq N$
  $F3 \leftarrow \varepsilon_3 \geq N$ **AND** $\varepsilon_1 \geq N$
else if $(D > 2/3$ **AND** $D \leq 1)$ ***then***
  $F1 \leftarrow \varepsilon_3 \geq N$
  $F2 \leftarrow \varepsilon_1 \geq N$
  $F3 \leftarrow \varepsilon_2 \geq N$
end if

Fig. 6. Pseudocode for fault identification and localization

Figure 7 shows the proposed open-switch switch fault detection algorithm block diagram. The actual measured input current slope sign S_{iL} is calculated by passing the input current derivative via a sign block. This algorithm depends on the input current i_L, and therefore does not require additional sensors in the system, which is intriguing because additional sensors can impact the system reliability, cost, and weight. The error counter signals are reset at the start of each switching period. The algorithm can detect faulty switch after one switching period, however, an additional switching period would be required for fault detection if the fault occurred later in the analyzed period. As a result, the minimum time for fault detection can be lower than one phase switching period and the maximum detection time is lower than two switching periods. The interleaved

DC–DC buck converter can use this fault detection approach also since it has the same waveform as that seen in Fig. 5.

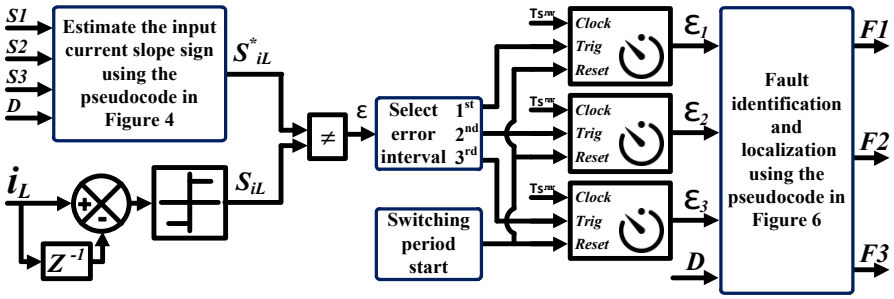


Fig. 7. Open circuit switch fault detection algorithm block diagram

3.3. Fault-tolerant control

Figure 8 shows the fault tolerant topology with redundancy for the PV system under study. The fault tolerant topology is achieved by connecting a redundant switch to each phase of the interleaved converter via a triac. In the event of a power switch failure in the interleaved DC–DC converter, the fault detection algorithm detects and locates the faulty switch and replaces it with the redundant switch *Tr* and activate the corresponding triac of the faulty switch phase. Moreover, the switching signal of the faulty switch is applied to the redundant switch.

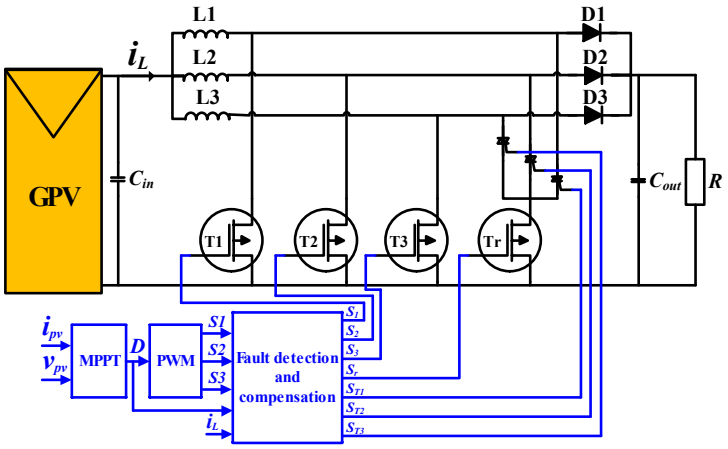


Fig. 8. Fault tolerant topology block diagram

4. Results and discussion

The PV system is developed and simulated using the Simscape Power Systems toolbox in the MATLAB/SIMULINK environment to validate the reliability of the proposed fault detection algorithm and fault tolerant control, as shown in Fig. 9. The control and fault detection algorithms

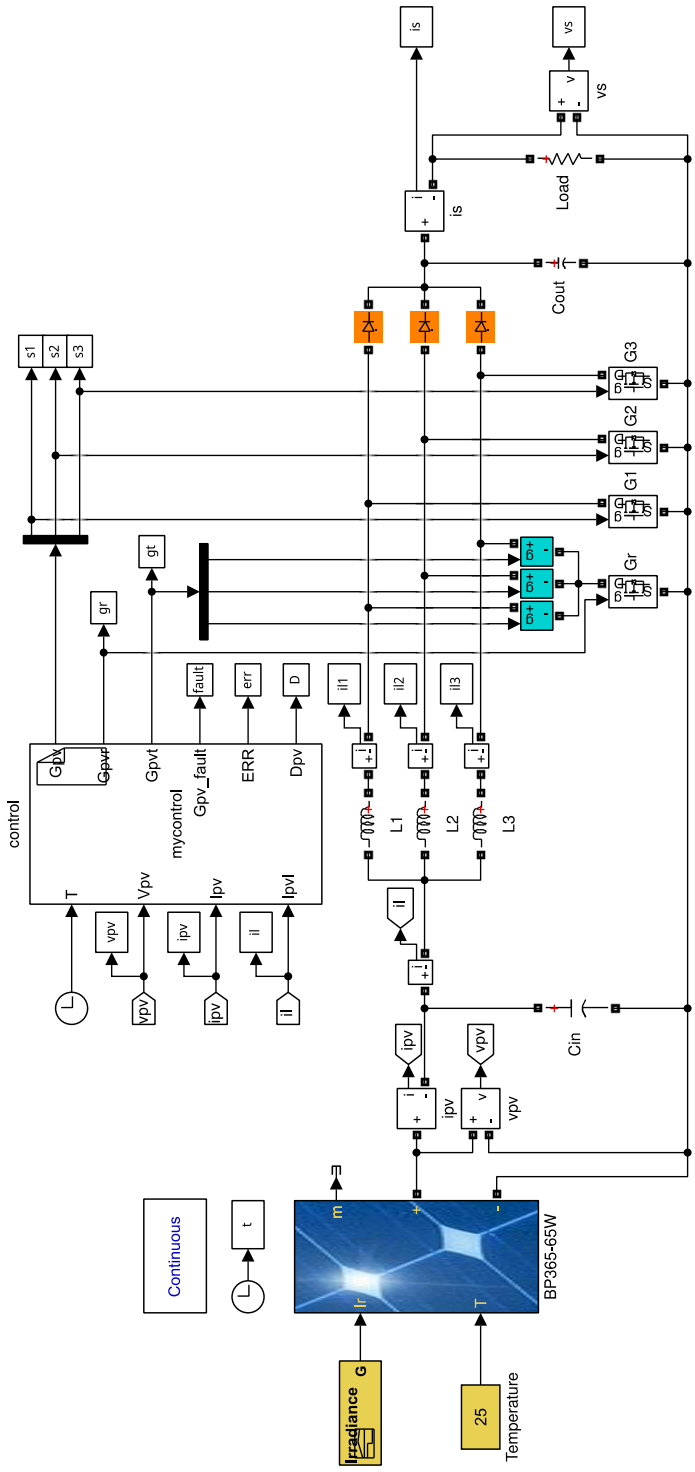


Fig. 9. PV system Simulink model block diagram

were written using "C" programming language. The simulation sampling period is set to 1 µs and the error threshold N is set to 30. The MPPT control technique sampling time is set to 1 ms with a 0.005 step size.

As seen in Fig. 10, the solar irradiation varies between 200 W/m^2 and 1 000 W/m^2.

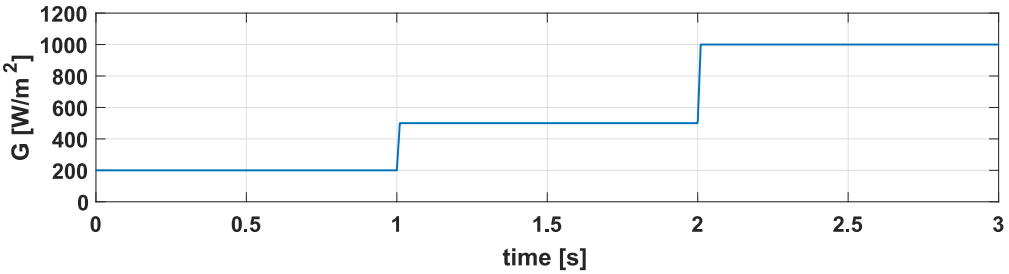


Fig. 10. Solar irradiation

In Fig. 11, the PV output current i_{pv}, voltage v_{pv}, power p_{pv}, and the duty ratio are shown. These obtained results demonstrate that the PV system is extracting the maximum amount of power from the PV array, which confirms that the P&O MPPT control is operating appropriately.

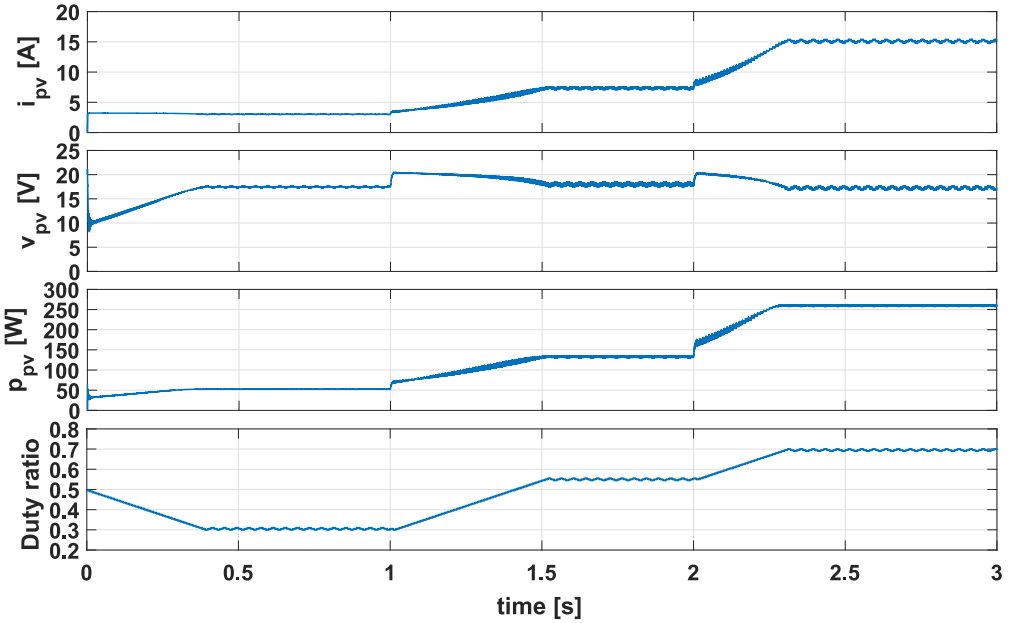


Fig. 11. PV system output current, output voltage, output power and duty ratio

Figure 12 shows the PV system output results when an open-switch fault occurs in switch $T2$ at $t = 0.6$ s without the fault tolerant control for a duty ratio values between $\frac{1}{3}$ and $\frac{2}{3}$ $\left(\frac{1}{3} < D < \frac{2}{3}\right)$.

As can be seen, after an open switch fault, the inductor current i_{L2} continues to decrease until it reaches zero resulting in a significant ripple increase to the input current i_L. The inductor current i_{L3} is increasing to compensate for the decrease in the inductor current i_{L2}. Consequently, the PV output current, voltage, and power also experience an increase in ripple. Nevertheless, despite these ripples, the system continues to function and quickly recovers to its maximum power point, as indicated by the transition in duty ratio.

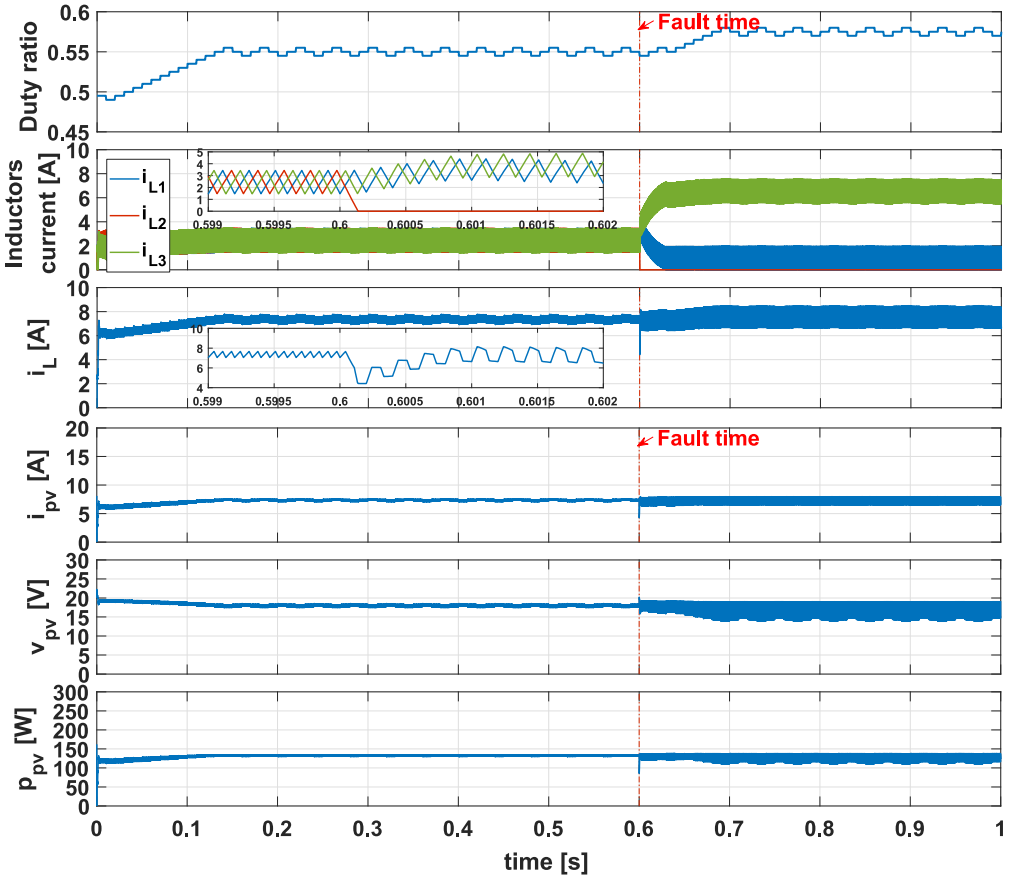


Fig. 12. Simulation results of open-switch fault occurrence in $T2$ without fault tolerant control for $\frac{1}{3} < D < \frac{2}{3}$

Figures 13, 14 and 15 show the fault detection algorithm signals when an open-switch fault occurs in switch $T2$ at $t = 0.6$ s for different duty ratio values ($D < \frac{1}{3}$, $\frac{1}{3} < D < \frac{2}{3}$, and $D > \frac{2}{3}$, respectively). The fault is detected after 95 µs for a duty ratio lower than $\frac{1}{3}$, when the error counter signal for the second interval is greater than the counting time $\varepsilon_2 \geq 30$ (as shown in Fig. 13). As can be seen in Fig. 14, the fault is detected after 162 µs for a duty ratio between $\frac{1}{3}$ and $\frac{2}{3}$, when the error counter signals for the second and third intervals are greater than the counting time

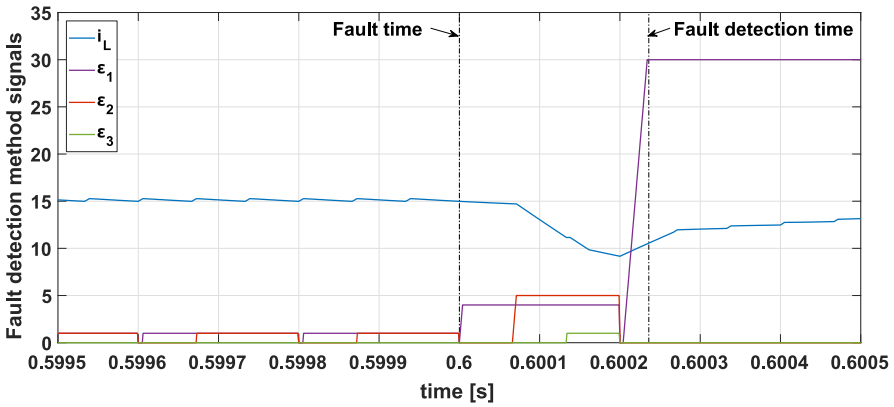


Fig. 13. Fault detection algorithm signals of open-switch fault occurrence in $T2$ for $D < \frac{1}{3}$

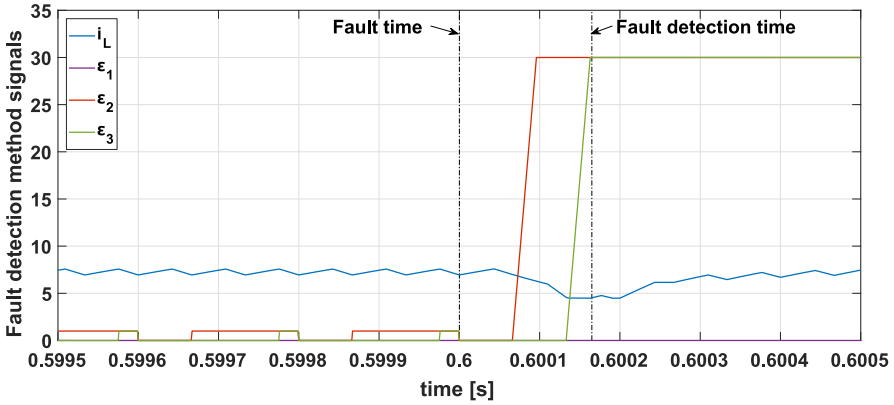


Fig. 14. Fault detection algorithm signals of open-switch fault occurrence in $T2$ for $\frac{1}{3} < D < \frac{2}{3}$

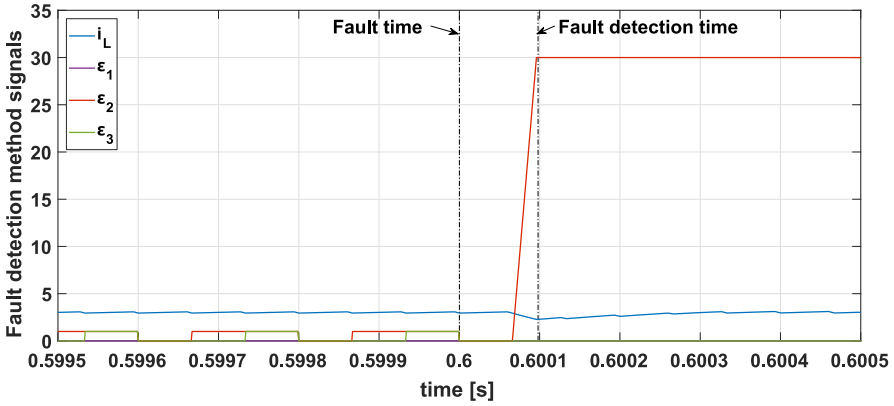


Fig. 15. Fault detection algorithm signals of open-switch fault occurrence in $T2$ for $D > \frac{2}{3}$

($\varepsilon_2 \geq 30$ and $\varepsilon_3 \geq 30$). For a duty ratio of more than $\frac{2}{3}$, the fault is detected after 233 µs, when the error counter signal for the first intervals is greater than the counting time $\varepsilon_1 \geq 30$ (as seen in Fig. 15). The minimum time for fault detection is lower than one switching period (200 µs) and the maximum detection time is lower than two switching periods (400 µs).

These obtained results demonstrate the efficiency of the fault-detection algorithm under different scenarios and for different duty ratio values.

Figure 16 shows the PV system output results under the same open-switch fault as in Fig. 12 when the proposed fault-tolerant control is implemented. These results demonstrate that the PV system continues to function normally after a brief transient. As can be seen in Fig. 14, the fault is detected at $t = 0.600162$ s, which is 162 µs after the fault has occurred and lower than one switching period (one switching period is 200 µs for 5 kHz switching frequency). The fault is detected when the error counter signals for the second and third intervals are greater than the counting time ($\varepsilon_2 \geq 30$ and $\varepsilon_3 \geq 30$), which corresponds to the criteria for power switch failure in $T2$ for a duty ratio between $\frac{1}{3}$ and $\frac{2}{3}$ specified in Table 4.

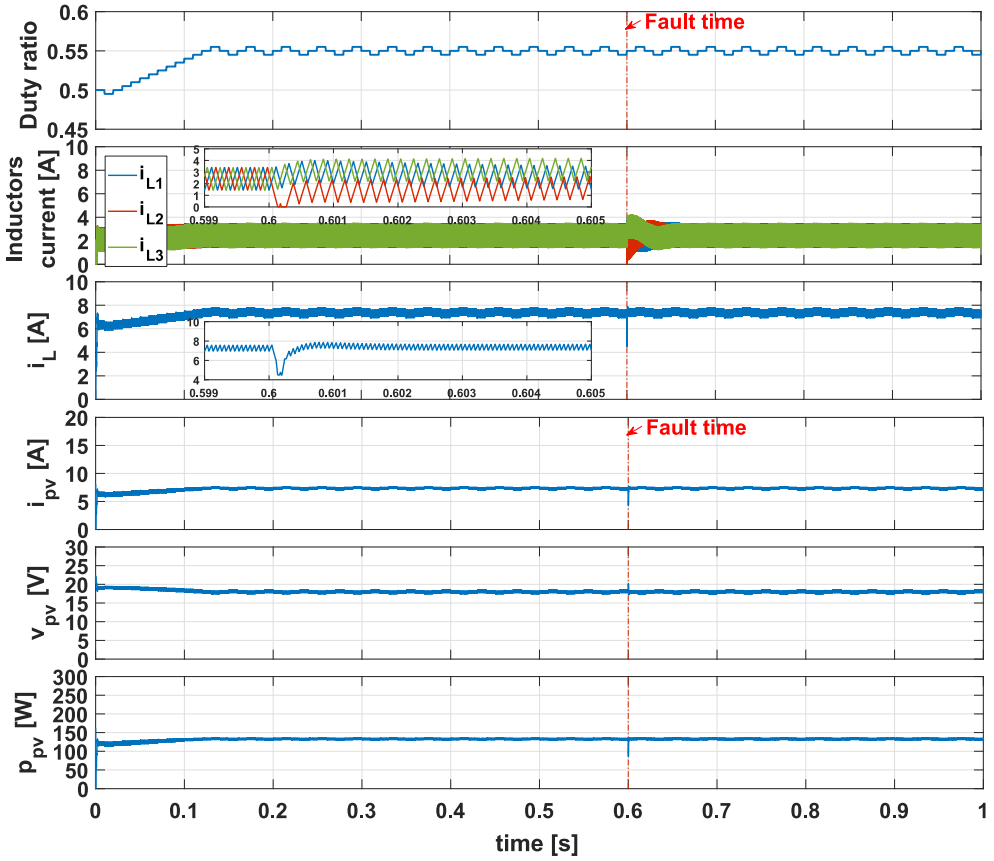


Fig. 16. Simulation results of open-switch fault occurrence in $T2$ with fault tolerant control for $\frac{1}{3} < D < \frac{2}{3}$

5. Conclusions

This paper has presented an open-switch fault detection algorithm for a three-phase interleaved DC–DC boost converter in a photovoltaic system. The fault detection algorithm depends on the input current slope sign, and therefore does not require additional sensors in the system. The fault tolerant topology was achieved by connecting a redundant switch to each phase of the interleaved converter via a triac. The obtained results show that the PV system can continue to function normally even after an open-switch fault occurs, demonstrating the viability of the proposed fault detection algorithm and fault tolerant control. In further research, it might be possible to enhance the fault tolerant control by readapting the interleaved converter to use only healthy phases. Further experimental tests would help us to verify the proposed fault detection algorithm and fault-tolerant control.

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