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A current-source concept for fast and efficient driving of silicon carbide transistors

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Abstract: The paper discusses the application of the current-source concept in the gate drivers for silicon carbide transistors. There is a common expectation that all SiC devices will be switched very fast in order to reach very low values of switching energies. This may be achieved with the use of suitable gate drivers and one of possibilities is a solution with the current source. The basic idea is to store energy in magnetic field of a small inductor and then release it to generate the current peak of the gate current. The paper describes principles of the current-source driver as well as various aspects of practical implementation. Then, the switching performance of the driven SiC transistors is illustrated by double-pulse test results of the normally-ON and normally-OFF JFETs. Other issues such as problem of the drain-gate capacitance and power consumption are also discussed on the base of experimental results. All presented results show that the current-source concept is an interesting option to fast and efficient driving of SiC transistors.

Key words: silicon carbide transistors, gate drivers, current-source, switching process

1. Introduction

A study of the papers regarding various types of Silicon Carbide transistors [1-5] leads to two main conclusions. At first, a very rapid development in this technology can be noted which has moved SiC transistors from promising novelty to recognizable, commercialized part of the power semiconductors industry. The second conclusion is that every type of the SiC transistor: MOSFET, JFET or BJT requires special attitude on the gate driver in order to fully utilize the performance of the device. This, obviously, result in a number of a gate/base driver solutions proposed in the last years [6-10].

The basic demand of the gate driver for a SiC transistor is good dynamics of the switching process. Fast changes of the current/voltage waveforms lead to low amount of switching energies what results in low switching power losses. In practice the rapid gate current peaks are required to recharge the input capacitance of the devices. This may be usually achieved with a standard totem-pole driver as in the Si MOSFETs or IGBTs case. Unfortunately, the recom-

mended voltage supply is asymmetrical in most cases (for instance MOSFET: +22/−5 V, normally-ON JFET: 2.5/−15 V, normally-OFF JFET +5 V/−12 V) and the generated current peaks at turn-on and turn-off are different. Furthermore, the low positive (i.e. 2.5 V) or negative (i.e. −5 V) supply voltage is usually not sufficient to ensure suitable dynamic. That is why special solutions of the gate drivers have been presented in the literature [6-8, 10]. Most of them use the capacitor to speed-up the switching process by means of more dynamic gate current peak. This solution is simple and results in a significant performance increase but some drawbacks may be also pointed out. At first the capacitor must be discharged after each switching action in some of existing RC circuit what takes time and result in duty time limitation. Moreover, the capacitor applied in the gate creates LC circuits together with parasitic inductances of the printed-circuit board (PCB) and device package. During the transients such as the transistor turn-on or turn-off, this circuit tends to oscillate in the MHz range.

Other possible solution which may be applied to achieve enough fast current peaks is a current-source originally proposed for the gate driver of Si MOSFETs [11]. The basic idea is to store energy in a magnetic field of a small inductor and release it into the gate of the driven transistor. The advantage is that even low voltage may be enough to create necessary current peak. Thus, asymmetrical supply is no longer a problem. Furthermore, high-frequency resonances may be avoided as the introduced passive element is inductive type and parasitic LCs are not introduced.

In this paper the gate drivers for the SiC transistors with the use of the current-source concept are discussed. Section 2 describes operation principles of typical current source while Section 3 deals with practical implementation in the gate drive circuit. Then, following Sections 4 and 5 show application of the current-source concept for the driving of normally-OFF and normally-ON SiC JFETs. Power consumption of the current-source drivers is discussed in Section 6 and the paper is concluded in Section 7.

2. Current source principles

The main SiC transistor may be represented by the standard model – see Figure 1a where gate circuit is composed by diodes and non-linear capacitances between gate, drain and source. Fast switching of the transistor may be only achieved when the capacitances of the device are recharged quickly and the gate driver should be capable to deliver dynamic current peaks.

The essential part of the discussed in this paper gate driver with the dynamic current source (see scheme in Fig. 1a) is a storage element: an inductor [11, 12]. In presented example the current-source is applied to generate positive current peak necessary at turn-on of the main transistor. This means that the positive voltage V_{CC} is not enough high to turn-on transistor fast with the typical totem-pole configuration (i.e. for normally-ON JFET V_{CC} is zero or in the range up to 3 V). The inductor L_R is connected between the positive supply V_{CC} and the driver output – the gate connection. After the rising edge of the driver control signal IN (see in Fig. 1b) the series switch T_1 is turned-on at time t_A. The sum of the voltages V_{CC} and V_{EE}

applied to the inductor L_R leads to a linear increase of the current i_{LR} as the switch T_3 is in on-state. At a certain instant when the inductor current has reached the desired peak value I_{LRP} (t_B), the switch T_3 is turned off. This breaks current path to the negative pole V_{EE} and the inductor current is now conveyed into the gate of the driven transistor. Obviously, this current commutation requires some time due to existing parasitic inductances of the gate driver as well as the transistor package but finally the gate current equals to the inductor current at t_C.

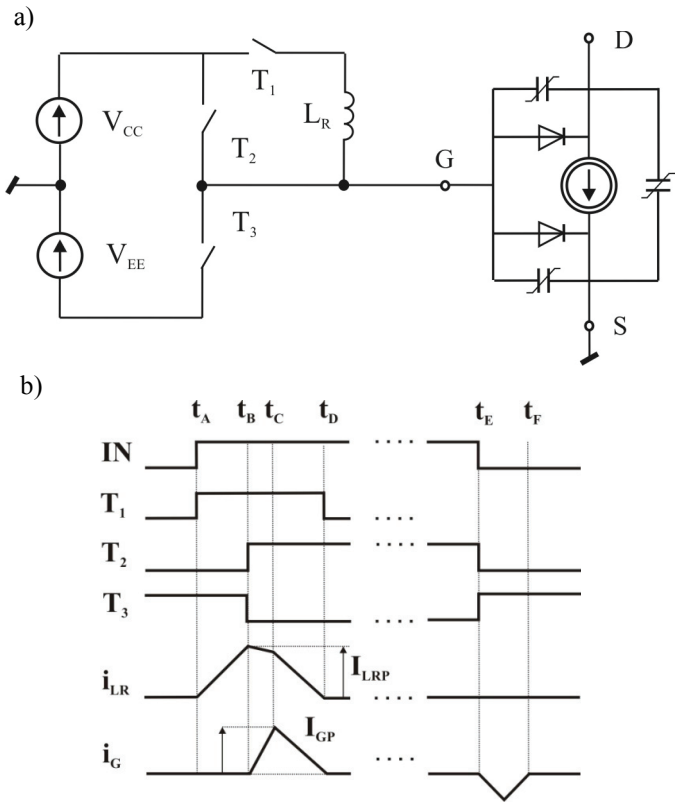

Fig. 1. Scheme of the gate driver with a current source applied to generate the current peak at turn-on (a) and the basic operation principles (b)

Then, the inductor and gate current start to fall as the switch T_3 is turned-off but there is no doubt that the main transistor has been already turned-on at t_D when T1 may be turned off. The switch T_2, which has been in on-state since t_B applies the positive voltage to the GS junction in the steady-state and may be utilized to deliver the gate current if necessary (i.e. normally-OFF JFET). In discussed case, the negative voltage V_{EE} is sufficient to ensure good dynamic of the turn-off process and, therefore, the current-source is inactive during turn-off. The use of the current-source at turn-off is also possible after changes in the circuit. Moreover, the inductor may be switched adequately to generate current peak either at turn-on and turn-off as can be seen in [12]. In the author opinion, however, the current-source as more complicated solution

should be only applied when positive or negative supply voltage is not enough high to ensure required switching speed. Thus, the current source is inactive in presented case and transition between T_2 and T_3 at t_E leads to discharging of the device capacitances by negative gate current. Finally, at t_F the device is turned off with negative GS voltage which equals $-V_{EE}$.

3. Practical implementation

As was mentioned above, the driver with the current source becomes more complicated in reference to the standard solutions based on the totem-pole pair. The inductor and one switch more are required but also special control sequence need to be generated. Thus, the practical implementation should be as simple as possible and common electronics components applied if the current-source driver is expected to be competitive solution.

Example of the current-source driver for normally-OFF JFET is presented in Figure 2. Two fast, low-resistive totem-pole drivers, IXD614, are applied to introduce the current-source principle as can be seen in Figure 2a. The upper branch contains series diode (low voltage Schottky) in order to eliminate lower transistor of the totem-pole (T_4) and use only T_1. In consequence, the branch with the inductor L_R generates only positive gate current pulses supplied from V_{CC}. The second totem-pole driver is utilized to deliver the steady-state gate current during the conduction stage of the main JFET. When T_2 is on, the current flows from V_{CC} to the JFET gate while the R_G resistor determines the amplitude (usually around 200 mA is required [7]). Finally, T_3 is turned-on when the main transistor is expected to turn-off under negative voltage V_{EE} = 12 V. Usually, maximum possible switching speed is required but it may be reduced by application of the optional resistor R_G'.

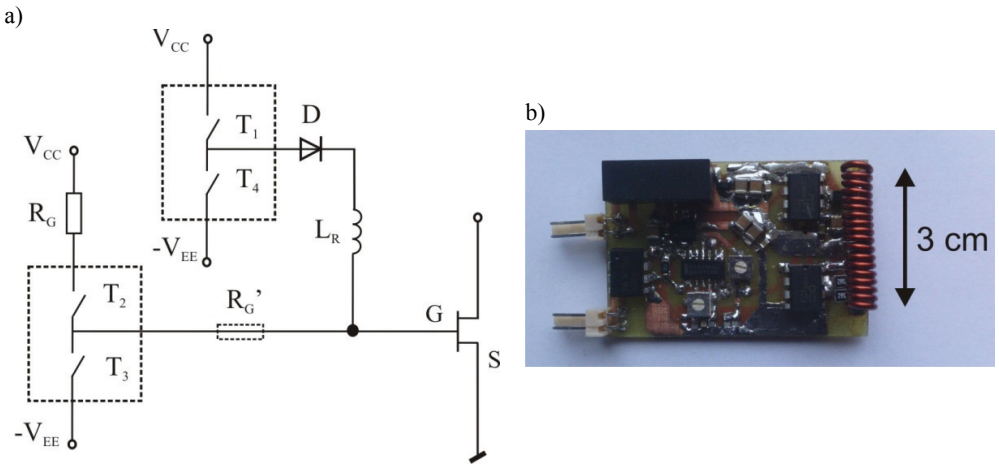

Fig. 2. Scheme (a) and photo (b) of the current-source driver for normally-OFF JFET implemented with two totem-pole drivers (size 35×50 mm, V_{CC} = 5 V, V_{EE} = 12 V, R_G = 10 Ω)

The inductor L_R was designed without a core (or just with air-core, Fig. 2b) taking into account operation conditions (short current peaks). The saturation current of this design is high, but the simplicity is also important benefit. The number of turns was experimentally determined to be 15 while the inner diameter of the inductor was approximately 3 mm. As can be seen in Figure 2b, the physical size of the inductor L_R is comparable to other electronics parts of the circuit. The inductance value, less than 200 nH, was chosen to be one order of magnitude higher than the expected parasitic inductance of the TO-247 package. Then, the amount of the stored energy is enough high to effectively built-up the gate current peak. It is the opinion of the authors, that this type of inductor design may be more reliable and stable than the speed-up capacitors [6, 8, 10] what can be counted as another advantage of the current source driver.

Another crucial part of the current-source driver is a logic block which is necessary to obtain the control signals sequence presented in Figure 1b. As three switches T_1 – T_3 are parts of two totem-pole drivers (Fig. 2a), only two control signals are basically required. The control signal of T_1 (upper totem-pole) is a short high-state pulse triggered by the rising edge of the input signal IN. The second required signal for T_2/T_3 equals the signal IN with a delayed rising edge (Fig. 1b). The delay of the control signal T_2/T_3 and the width of the T_1 pulse are expected to be adjustable in order to shape the gate current peak.

After suitable design procedure the logic block with only four 2-input NAND gates (single integrated circuit, i.e. 4011) and two RC delay circuits is employed, as can be seen in Figure 3. Changing the time constant R_1C_1, the duration between times t_A and t_B is adjusted (see Fig. 1b). This means that the rise time of the current through L_R can be changed. The second delay circuit R_2C_2 controls the T_1 pulse width (between t_A and t_C). Obviously, the R_2C_2 time constant should be longer than R_1C_1 to set the duration between t_B and t_C, necessary to build up the peak of the base current as can be seen in the sequence presented in Figure 1b.

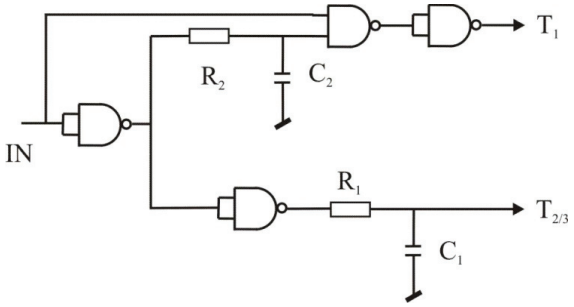

Fig. 3. Schematic of the current-source driver for normally-OFF JFET implemented with two totem-pole drivers

4. The current-source driver for the normally-ON JFET

The normally-ON JFET, due to negative threshold voltage, is in on-state without any gate bias what is usually recognized as main drawback of this device from the system safety point of view. On the contrary, a gate driver become simpler as may successfully operate with only negative supply. It is also possible to apply slight positive voltage, lower than built-in voltage

of the GS junction, in order to reduce the on-state resistance but this makes the supply bipolar again. But this voltage may be not enough high when the dynamic current peak is required to turn-on the JFET fast. This is the case of the dual-gate trench JFET discussed in [13]. This type of SiC transistor offer very low specific on-state resistance (3 mΩ cm^2), which is accomplished by significant input capacitance, especially existing between the drain and gate. In consequence, a typical totem-pole gate driver with the positive supply of 2.5 V is not capable of recharging the device and turn on process is extended in the time [13]. This is exactly the situation when the current-source driver is a perfect solution to speed-up the switching process of the normally-ON JFET. Basically, the circuit shown in Figure 1a is suitable to improve the transistor performance [13] but extended version with an extra positive voltage supply is also interesting possibility – see scheme in Figure 4. This positive supply is applied to higher voltage across the inductor L_R during the current rise phase (between t_A and t_B in Fig. 1b). In result, the time period necessary to store energy in the inductor is shorter and higher values of current peak I_{GP} are available. This solution seems to be more complicated in reference to circuit in Figure 1a but in practice the isolated dc/dc converter with double output (i.e. 2×15 V) is required to supply both drivers. The only difference is that in the gate driver from Figure 4 two voltages are employed: high V_{CCH} = 15 V and the converted (by linear regulator or dc/dc converter) low voltage V_{CCL} = 2.5 V. In the solution from Figure 1a only lower voltage of 2.5 V is necessary but is usually converted from 15 V anyway.

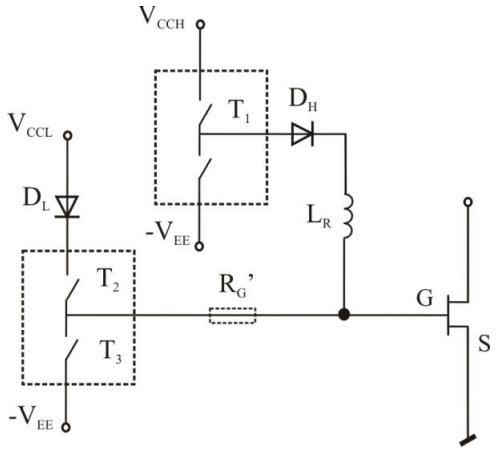

Fig. 4. Scheme of the current-source driver for normally-off JFET implemented with two totem-pole drivers

The current-source driver was applied to control the DGT-JFET tested under a standard double-pulse procedure according to schematic in Figure 5. The transistor with chip size of 15 mm^2 rated at 1200 V was switched with the 1200 V/30 A SiC Schottky diode. Waveforms during turn-on and turn-off processes were recorded with digital oscilloscope – see Figure 6. The turn-on process presented in Figure 6a shows very good dynamic performance of the controlled transistor due to applied in the gate circuit current-source. The current peak in the range of 5 A which is applied to the JFET gate terminal with an overvoltage (around 40 V) leads to turn-on time lower than 80 ns (600 V/15 A). The turn-on time of the same device controlled with totem-pole driver was counted in microseconds as can be found in [13], so the

achieved performance improvement is noticeable. The current rises with di_D/dt around 1.25 kA/μs and, what is more important for this device, the drain-source voltage falls with the speed around 12.5 kV/μs. The waveforms allow estimation of the turn-on energy which is around 350 μJ. The turn-off process observed for the same conditions (Fig. 6b) takes approx. 120 ns but the amount of the energy loss is lower (300 μJ).

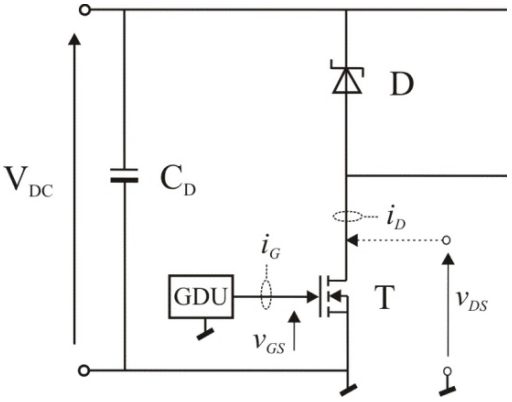

Fig. 5. Schematic of the double-pulse setup applied to test the switching performance of the transistor/diode pair

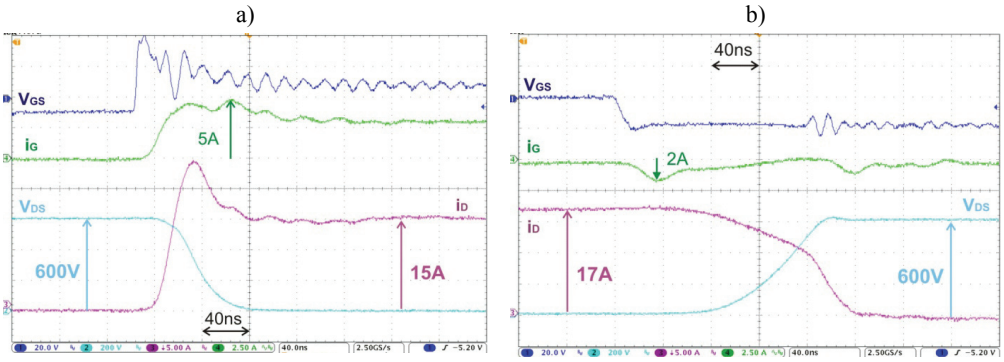

Fig. 6. Switching process of the DGT JFET with CS driver: turn-on (a) and turn-off (b)

5. Current-source driver for the normally-off JFET

The current-source concept in the gate driver circuit of SiC devices was firstly presented for bipolar transistor [12]. Besides rapid current peaks this device requires a steady-state base current during conduction stage and this exactly the same what is expected from the gate driver circuit of the normally-OFF (enhanced mode) SiC JFET [7]. Thus, the current-source driver (schematic in Fig. 2) originally designed for BJTs was employed to drive normally-off SiC JFETs (SJEP120R100) which were operating in the bridge leg.

The switching performance of the devices was again verified by means the double-pulse test (schematic in Fig. 5). Waveforms of the gate current, drain-source voltage and drain cur-

rent presented in Figure 7 show the turn-on and turn-off process. Both may be described as very fast as turn-on time is around 35 ns and turn-off time is slightly above 20 ns. The turn-on current peak conveyed into the gate terminal is up to 8 A what results in quick drain-gate capacitance discharge and very rapid drain-source voltage fall (~50 kV/μs).

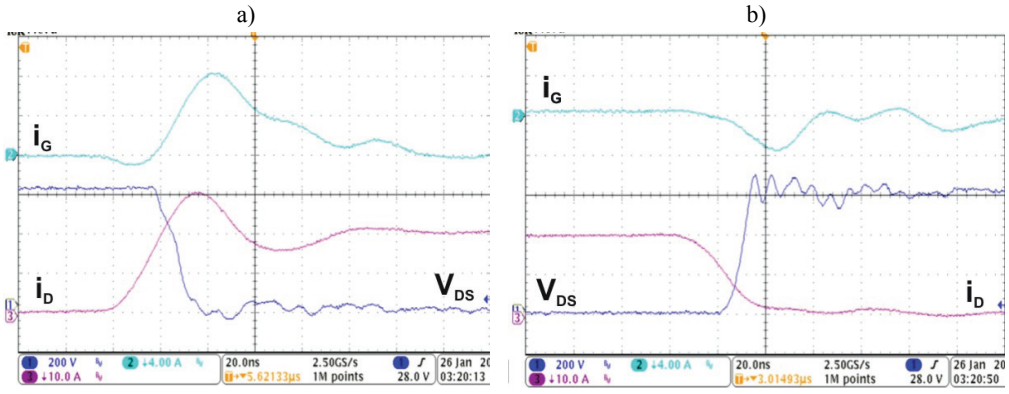

Fig. 7. Turn-on and turn-off of the DGT JFET with CS driver: turn-on (a) and turn-off (b)

The operation of the transistors in the bridge leg, as can be for instance seen in Figure 8, requires special attention on the gate driver especially when devices switch very fast. The problem is basically caused by drain-gate capacitance. Let us assume the direction of the current i_O to the T_1/T_2 bridge leg from the transformer during transition from T_2 to T_1. After turn-off of the transistor T_2 the current is conveyed to the anti-parallel diode of the T_1 and the potential of the middle point is switched from close to zero to close to U_{DC}. This means that some current flows from the gate to drain of T_1 as the nonlinear capacitance C_{GD} must be discharged. This current may cause some negative effect in the driver. There is a risk of an accidental turn-on of T_1 caused by the voltage drop on the gate resistor and, therefore, low resistive path for drain-gate current must be ensured. Behaviour of the current-source drivers controlling T_1 and T_2 is presented in Figure 9 where waveforms of the gate-source voltages

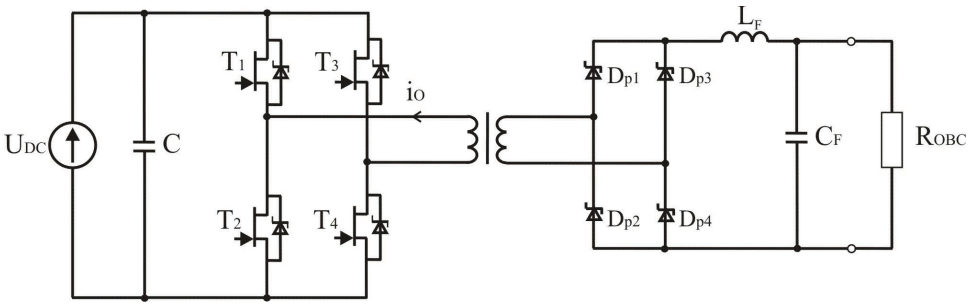

Fig. 8. Single Active Bridge (SAB) converter with normally-OFF SiC JFETs

and gate current of upper and lower transistor are visible. When the DC supply voltage is disconnected, the middle point potential does not change and only the 2 A current peak is observed (recharging of C_{GS}) – see Figure 9a. After the increase of the DC voltage to 600 V the current from the drain reaches 8 A (Fig. 9b) as the drain-gate capacitance is recharged. In spite of this current the gate source voltage remains at safe distance from the pinch-off voltage (~1 V) and device is kept in off-state.

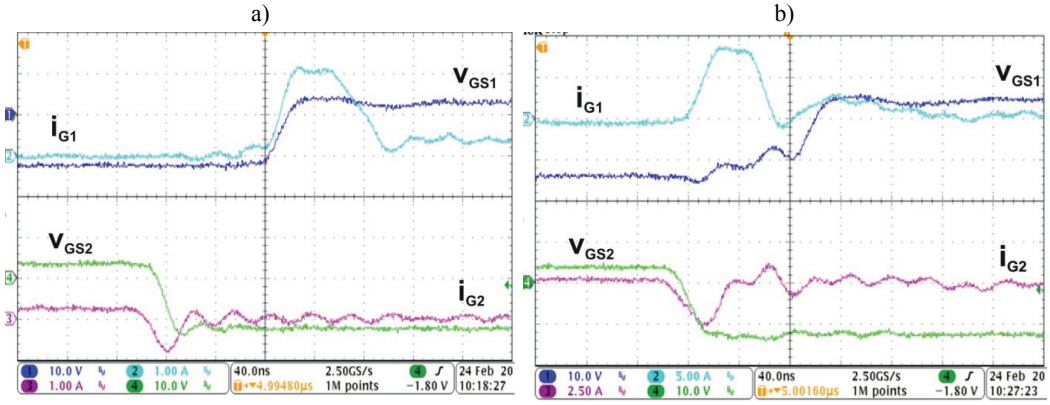

Fig. 9. Waveforms of the gate-source voltages and gate currents of the single transistor legs during the switching from T_2 to T_1 when: a) $U_{DC} = 0$ V and b) $U_{DC} = 600$ V

6. Power consumption of current-source driver

The power consumption of the current-source driver will be discussed with the use of example of the bipolar transistor. The circuit from schematic in Figure 2a was applied to drive 1200 V/6 A BJT [12], which requires 320 mA of the steady-state current to conduct the collector current. The driving conditions are similar to presented in [10] (100 kHz, 50% duty ratio) and, therefore, types of power losses are almost the same. Most of the power losses are caused by the steady-state current on the base-emitter junction and base resistor R_G. As the positive supply is $V_{CC} = 5$ V, the instantaneous power in steady-state is around 1.6 W but this amount is limited to 0.8 W due to 50% of duty ratio. On the other hand, this value has to be increased by the power losses in the auxiliary dc/dc converter (24 V/5 V) with efficiency around 85%. Another important part of the losses is caused by the dynamic current peaks on the base-emitter junction and is strongly dependent on their peak value and switching frequency. For the discussed example of the BJT amount of 220 mW was determined for the peak value of the current equal to 4 A and switching frequency of 100 kHz. This value should be again increased by the power losses in auxiliary dc/dc converter. As the current peak is mainly determined by negative supply, the measurement of the total power consumption for $V_{EE} = -15$ V, -5 V and 0 V was conducted. As expected the power loss decreases with the

negative supply and was 1.9 W, 1.6 W and 1.15 W respectively. The same measurements were also conducted for various switching frequencies (and $V_{EE} = -15$ V) – see results in Figure 10. Obviously, the power consumption rises with switching frequency but frequency independent component is noticeable. There is no doubt that some extra losses occur, such as losses in the logic circuit and especially in the linear regulator (15 V/5 V) as the TTL logic was applied.

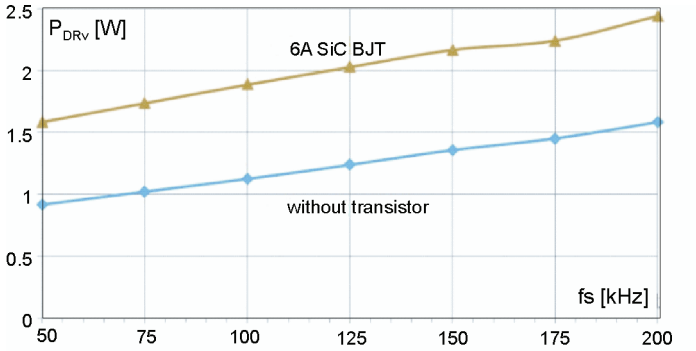

Fig. 10. Power consumption of the current-source driver measured for various switching frequencies for 50% duty ratio and 320 mA of the steady-state base current

7. Conclusions

The concept of the current-source applied in the drivers for SiC transistor was discussed in this paper. A simple current source with simple coreless inductor is able to generate the current peak which is thought to switch the main transistor very fast. In consequence the switching time and energy may be reduced significantly what may lead to operation at very high frequency or high efficiency. Very good switching performance was proved for various examples of normally-ON or normally-OFF JFETs. Correct operation in the bridge leg was also shown. Presented practical solutions of the current-source driver are slightly more complicated circuits than standard-solutions. Power consumption, what was presented on the example of the base driver for the bipolar transistor is on the same level. All in all, current-source driver is interesting option when fast and efficient of the SiC transistor is expected.

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