CMOS Readout Circuit Integrated with Ionizing Radiation Detectors

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Abstract—This paper describes the work performed in ITE on integration in one CMOS chip the ionizing radiation detectors with dedicated readout electronics. At the beginning, some realizations of silicon detectors of ionizing radiation are presented together with most important issues related to these devices. Next, two developed test structures for readout electronics are discussed in detail together with main features of non-typical silicon process deployed.

Keywords—readout electronics, ASIC, SOI, ionizing radiation detectors

I. INTRODUCTION

THE main objective of presented work was to integrate in one monolithic integrated circuit the ionizing radiation detectors with dedicated readout electronics. This work can be considered as follow-up of previously performed research [1], [2]. In previous solutions based on modification of the ITE proprietary silicon process using the SOI substrates, detecting junctions were manufactured below the buried oxide (BOX) in some kind of crater etched through the device layer. Relatively large dimensions of the crater resulted in the low level of layout compaction and in significant parasitic distributed capacitance. An important disadvantage of that solution was the influence of high voltage applied to cause the full depletion of detecting diodes to the readout electronics located in device layer – the back-gate effect in transistors. This can be minimized by utilization of thick device layer allowing use of classical bulk transistors, but in this case another negative influence is caused by P wells touching the BOX and changing the potential distribution under them, what interferes the charge collection process. The remedy is deployment of the SOI substrates with extremely thick device layer (to prevent the wells from touching the BOX). Such a solution, however, is hardly compatible with any foundry standard process [2]. In discussed work an advanced silicon process, namely H035 from IMS Duisburg (Fraunhofer Institute for Microelectronic Circuits and Systems in Duisburg, Germany), was used for non-typical purpose to provide the vertical integration of detecting junctions and readout electronics. As one option of this process the high-energy Boron implantation is deployed to manufacture the P-type area directly beneath the BOX, and

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W-plug contacts are used to connect it to the rest of the circuit located in device layer. This kind of junction (P+ implantation and n type, preferably high-resistive for detectors, handling wafer) was developed for the purpose of shielding the low-voltage sensitive electronics from the influence of HV devices integrated into the IC. For that reason this high-energy doping process layer is named as SHIELD implantation. The main idea of discussed solution was to use the SHIELD implantation in non-typical way – to deploy it for building the detecting junctions – pixels. Having the readout electronics (or its most sensitive parts) compact enough it would be possible to locate it directly above each pixel (readout electronics layout area should be close to pixel junction area) and to connect them together by W-plugs. In such a solution, the detecting junction would be utilized to shield the sensitive readout electronics from HV influence, to get rid of back-gate effect. To provide effective shielding, detecting junctions have to be kept at constant (or near constant) potential regardless of the charge collected, what in turn requires more advanced readout circuit architecture to be used – one based on a charge amplifier. Such a solution is discussed in further chapters of that paper. Figure 1 illustrates schematically detector cross-section in H035 process (on the right) and previous solution developed in ITE (on the left). This compact layout together with advantages of the new technology allows for more efficient read-out architecture than presented in [1].
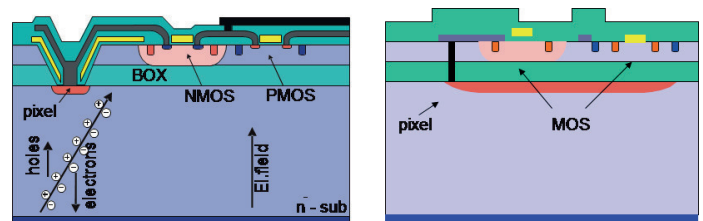

Fig. 1. Schematic crossection of detecting junction integrated with readout electronics in ITE process (left) and H035 process (right).

II. DEVELOPMENT OF TEST STRUCTURES

A. 1st Test Structure

The work was started with examination of usefulness of the H035 process, and in particular, the junctions made of SHIELD implantation. The first test structure consisted of four arrays of junctions in different configurations, dedicated to measure the quiescent (dark) current and resistance of contacts. The full characterization of mentioned junctions was not available from the foundry, because these elements were

(a) reverse direction   (b) forward direction
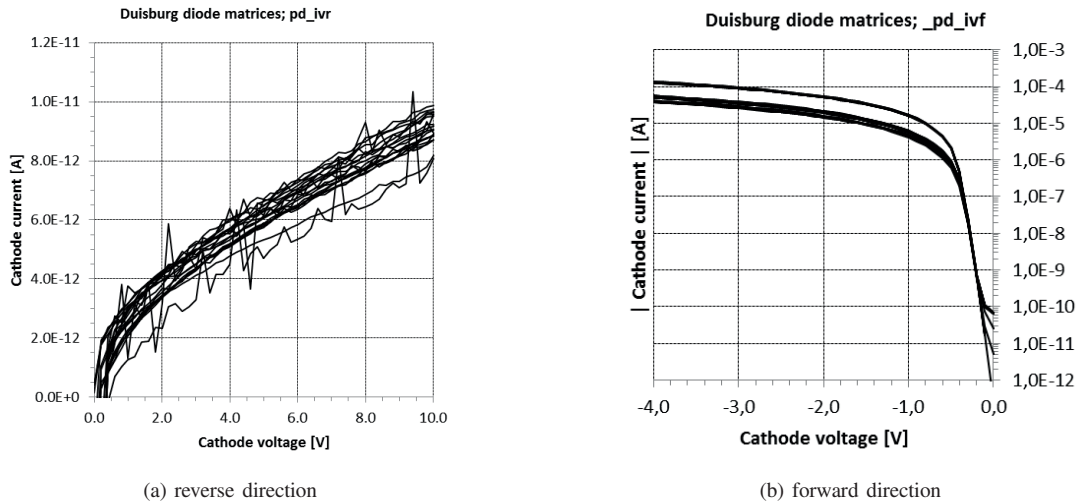
Fig. 2. Typical characteristics of the detecting junctions.

intended and used before only for shielding purpose, so their parameters were not too critical for any foundry design. The measurements were done on a number of test arrays available on a part of 200 mm wafer, each of them is made of 64 (8 x 8) junctions connected in parallel. The typical reverse and forward characteristics are shown in Fig. 2a and Fig. 2b respectively.

Forward bias characteristics exhibit a high on resistance (Fig. 2b), furthermore groups of devices exhibit different resistances. The diodes made of SHIELD implantation, despite their not-typical forward characteristics are very interesting and promising, due to very low value of the reverse currents, which enables their deployment in a function of detectors. The relatively high value of contact resistance is not a problem because the current flowing through the pixel is negligible.

Another part of test structure was the very simple readout circuit based on the source follower concept, with capacitive coupling at the input. This circuitry was expected to provide some comparison with previously used concepts, manufactured in different silicon processes during former research. Its schematic is presented in Fig. 3.
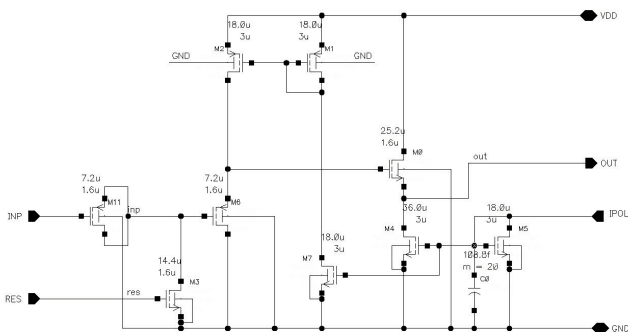

Fig. 3. Schematic of the simple readout circuit

B. 2nd Test Structure – Single Pixel Readout Circuit

After promising results of 1st test structure measurements it was decided to develop second, more complicated block – the readout circuitry for a single pixel. Unfortunately in the meantime the information was obtained from IMS, that H035 process variant with SHIELD implantation is out-of-use and the date of its next run is unknown. The MPW runs without this option were still available. Taking this into account it was decided to modify the circuit to enable the laboratory measurements with input signal coming from test setup, rather than from junction below the BOX.

The readout circuit for single pixel consists of following blocks:

1) Input circuit
2) Charge amplifier
3) Shaper
4) Peak detector
5) Auxiliary circuits

The input circuit was intended to provide the reverse bias for detecting junction, created of the SHIELD implantation layer. Due to temporary unavailability of this option in H035 process the input circuit was redesigned to enable measurements with input stimuli coming from external generator. To avoid problems related to stimulating the circuit with relatively short (10ns) current pulses, and the immunity of charge amplifier input (high resistance) to external disturbances and parasitic coupling from another input/ output signals it was decided to use the AC coupling (capacitive divider of 109fF to 445fF).In this manner it was possible to stimulate the circuit with square wave of several mV amplitude. Input signal from the divider is fed to the charge amplifier build on the PMOS differential pair (better 1/f noise parameters of P-type transistors) with voltage type parallel feedback based on two FETs. The gate of one of them working as resistor can be disconnected from the feedback loop and externally controlled using dedicated test signals. Such an option was introduced to enable the external change of circuit parameters during laboratory tests. The non-invering input of differential pair is biased with half of the
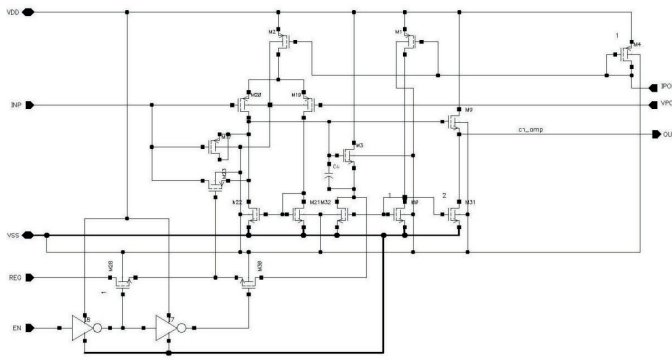
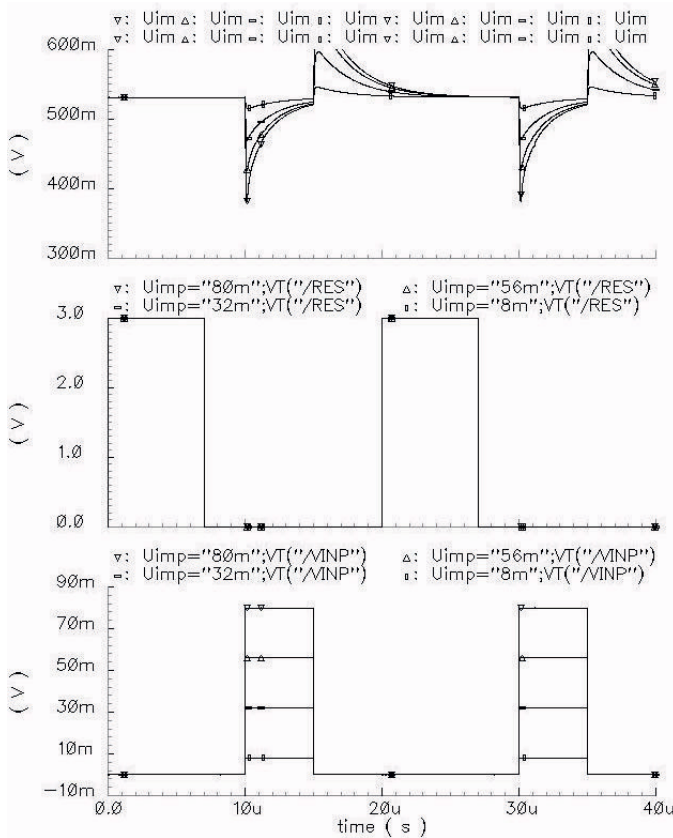Fig. 4. Schematic of the charge amplifier

Fig. 5. Transient response of the charge amplifier for voltage pulses of 8, 32, 56 and 80 mV.

supply voltage. Figure 4 presents schematic of the charge amplifier.

The voltage pulse formed within the charge amplifier (Fig. 5) as the response for charge pulse generated by detecting junction is passed to the shaper.

The role of this block is to transform it to the exponential form. It is done by the high side and low side bandwidth limitations, and the aim of this operation is improvement of the noise parameters of overall circuit. The shaper is designed in differential pair topology with voltage type resistive parallel feedback provided by long-channel PMOS (w=3.6μm l=10μm). In similar way as in charge amplifier, the non-inverting input is biased with a half of the supply voltage.

The frequency response and output pulse parameters are determined by: serial input capacitance, parallel capacitance, feedback loop resistance and parameters of the FET used as amplifier. There is a circuitry built in, similar as in the charge amplifier, which enables the gate of FET operating as resistor in feedback loop to be disconnected and controlled from outside using dedicated test signals. The output of the shaper (the source of the last follower) can be pulled low using one of three signals – master reset, shaper reset (individual) and the last one generated by the logic part of the circuit during processing of the received pulse. This constitutes the locking-down (disabling the signal path) functionality. The schematic of the shaper is shown in Fig. 6.

The role of subsequent block – the peak detector is to store the maximum (peak) value of the input signal (one coming from the shaper) as DC level until it is read by external circuit. The circuit is also designed in differential pair topology with current type output used to control the current mirror charging the "memory" capacitor (2.8 pF). The charging current of this cap is proportional to the difference between input voltage and the voltage across cap increased by VGS of the FET used as source follower separating the cap. Hence the cap is charged to the peak value of the input pulse, and the discharge process is possible only through the reset circuit. Unfortunately, data concerning the self-discharge rate for this kind of capacitor were not available during design phase. Another part of peak detector is mono-stable multivibrator, which is triggered by the amplified charging current of the "memory" cap. The 350ns long output pulse of multivibrartor denotes, that there was a charge pulse of at least 1000e level received at the charge amplifier input. The "memory" capacitor stores the peak value of the signal until reset. The voltage signal from "memory" capacitor via the source follower inside peak detector and the external buffer is available at the output of test chip. The digital block consists of several mono-stable and bi-stable multivibrators which are used to provide self-timing synchronization of previously described analog block. The output MEAS_EN level is changed from L to H approx. 360ns after the peak of the pulse from the shaper has appeared (which corresponds to 1.16 μs since the detecting junction excitation). This change denotes, that there is a DC signal ready for conversion awaiting at the analogue output. Another part of logic is responsible for blocking (locking-down) the signal path after reception of charge signal generated by one particle from being disturbed by signal generated by subsequent one. This functionality is switched by the ENA input of the chip – whenever it is high, the output of the shaper is tied below the 100mV which causes that pulses of amplitude lower than 1.6V are not transferred to the peak detector until reset. Setting ENA input to low disables signal path locking functionality described above. The schematic of the peak detector is shown in Fig. 7. The DC and transient simulation were performed in test circuit shown in Fig. 8. Figure 9 presents the results of parametric transient simulation for square pulse at the input with amplitudes of 8,32,56 and 80mV and rise time of 10ns (signals from the top: the peak detector output, the shaper output, input stimulus, reset). The relatively high non-linearity can be observed in this simulation, what is result of the
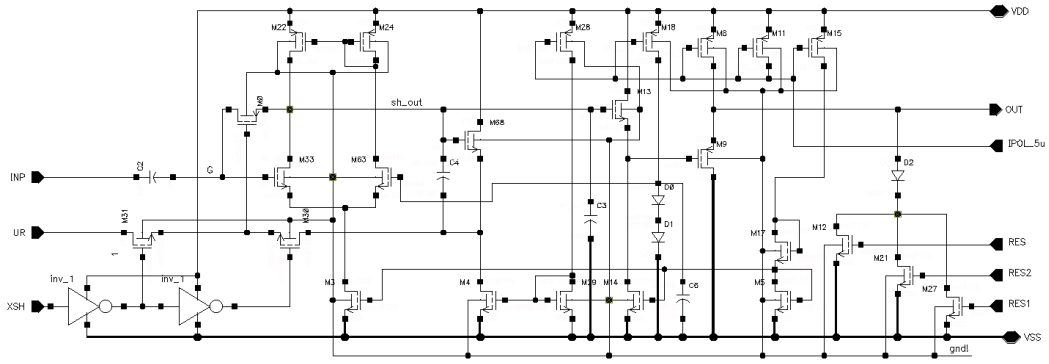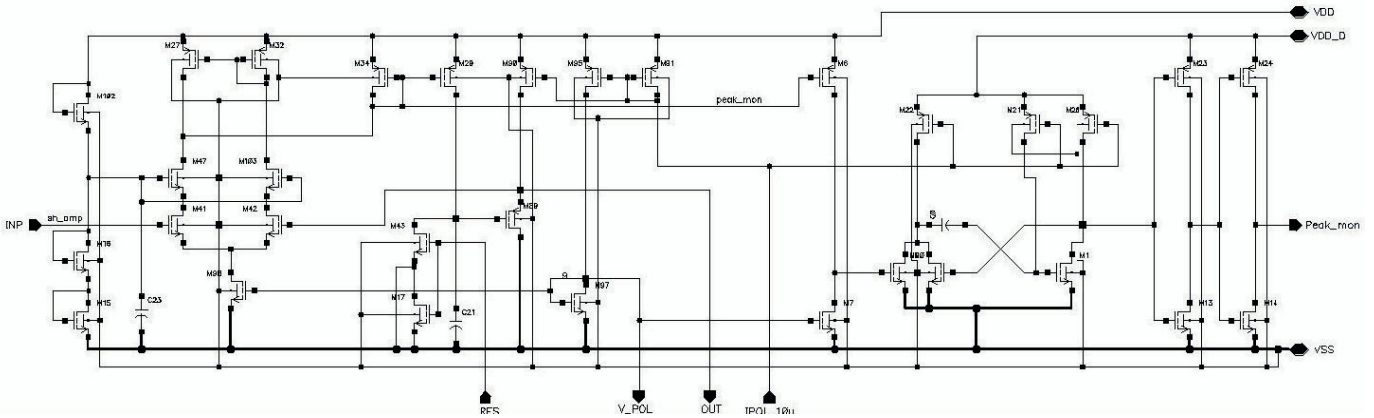
Fig. 6. Schematic of the shaper.
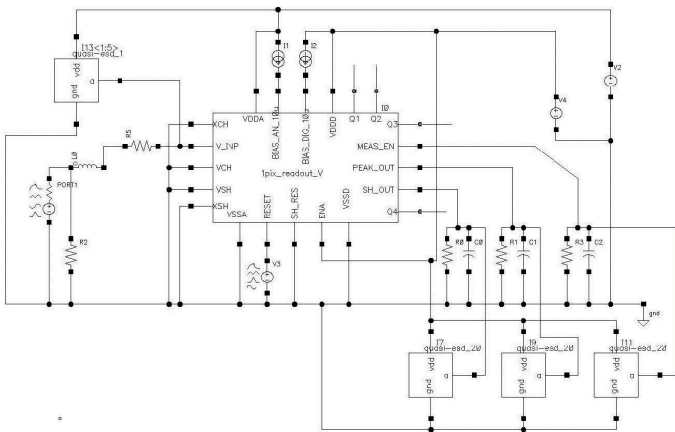

Fig. 7. Schematic of the peak detector.

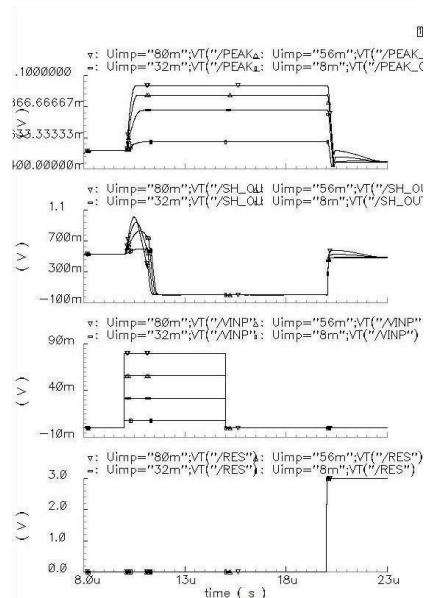Fig. 8. Schematic of the test bench used for simulation of single pixel readout circuit.

operating point of transistors (small currents) and deployment of FETs as high-value resistors. Another issue is lack of the linear (e.g. MIM) capacitor in the device set for H035 process.

This non-linearity cannot be eliminated in total by correction of FETs dimensions and operating points, so it was assumed that fine linearity correction will be performed in further stage by software. Figure 10 shows the results of measurements of manufactured testchip – the signals sequence

Fig. 9. Results of parametric simulation of single pixel readout circuitry for 8, 32, 56 and 80 mV stimulation amplitude.

starting from the top is: master reset, input, shaper output, peak detector output.
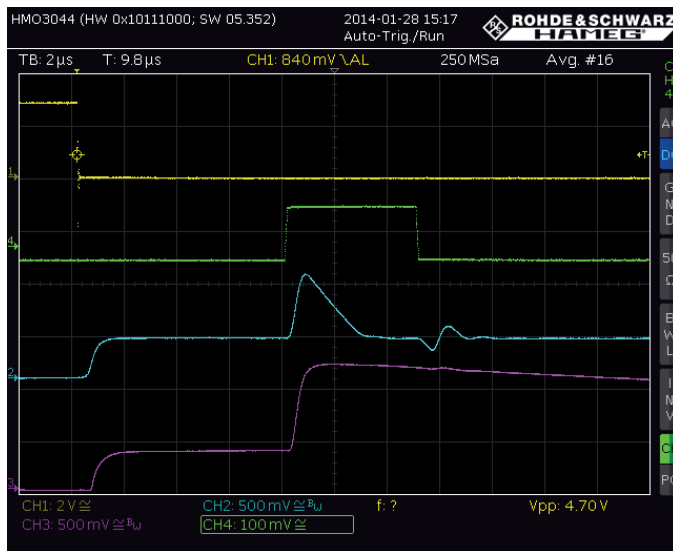
Fig. 10. Measurements results for manufactured testchip – single pixel readout circuit

III. EXTENDING THE FUNCTIONALITY OF PDK FOR H035 PROCESS

In parallel with development of the circuit itself another effort was spent to extend the functionality of Beta PDK for H035. The complete readout circuit for single pixel was considered to be complicated enough to require the operating layout verification suite as prerequisite, while there was only the first version of DRC available. This work was based on own experiences related to MPW service and PDK for ITE proprietary CMOS process development [3]. At the beginning, the Virtuoso-XL^{TM} (schematic driven layout in Cadence Design Systems toolset) was enabled to speed-up the layout drawing process by automated generation of parametric cells with properties set accordingly to the schematic. It required another section to be added to the technology file. In the next stage, the DRC procedures were debugged and modified according to the last available version of Design Manual for H035. Detection of each design rule violation was tested separately in dedicated layout. The most complicated task concerned the LVS procedures (in fact the extraction and comparison procedures). Among two possible device extraction concepts, based on advanced layer processing or on device recognition layers deployment, the first one was used as more flexible and, what's more important, not requiring the parametric cells to be modified. In a brief this method can be described as a series of operation on layers (geometric AND, geometric OR, searching for the butting shapes etc.) which results in all devices to be separated from the layout. For example, the channel of MOSFET is found as superposition (geometric AND operation) of active area (hole in LOCOS oxide), proper type of diffusion, polysilicon (gate). The drain and source areas are recognized as superposition of active area with proper type of diffusion, without the polysilicon (geometric ANDNOT operation) butting to previously defined MOSFET. The next part of extraction procedures deploys the measurement functions to determine the geometric properties of already found devices (like W and L of transistor) as

relations of its component layers. Such statements have to be defined separately for all devices available in the process. The comparison rule file contains set of procedures responsible for matching of one cell view (schematic) against another (extracted). One separate procedure is defined for each family of devices having the same specific set of parameter important for comparison (e.g. for all types of MOSFETS). Besides the comparison procedures the reduction and filtering ones are also usually defined in comparison rule file. The role of the first ones is to replace the set of one type components connected in series or in parallel by its equivalent circuit. This enables layouter to split one device (e.g. capacitor) into pieces to improve the silicon area utilization. Filtering procedures have been used to remove the unnecessary devices from the network. The pins of removed device can be shorted or left open depending on the function of removed component. Typical application of filtering procedures is to get rid of elements used in schematic for simulation purposes (e.g. definition of parasitic devices, patch cells). The LVS procedures testing process was performed in two stages. The first of them was to prove the parameter measurement functions within extraction procedures – it utilized some test layouts containing instances of process devices differing one to another with parameters set applied. The second stage was to check the comparison procedures against false positive and false negative type errors, starting with single instances of each type of device. After that, more complicated sets of devices were applied to examine the correctness of reduction rules. The usefulness of in-house rebuilt PDK was proved in 2012 during layout drawing for the 1-pixel readout circuit. Figure 11 shows the mistake
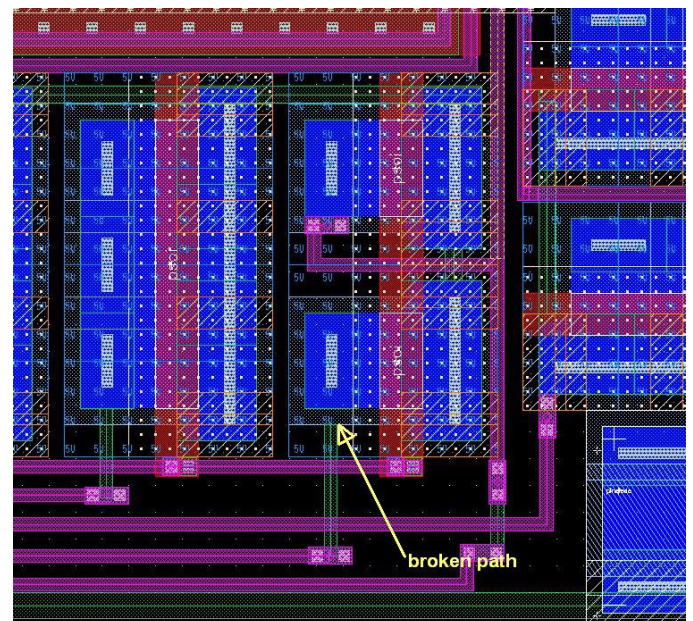

Fig. 11. The example of error in layout, very hard to find without the LVS procedures.

committed by layouter – the interconnecting path on first level of metalization became broken as a result of shifting the active device (transistor) while compacting the layout. Such a specific error is not detected by DRC – the distance between broken path and another shapes on the 1st metalization is

bigger than minimum. Moreover, this error is very hard to be detected "manually" by visible inspection of the layout. The only way of fast and reliable detection of such errors are LVS procedures.

IV. THE FIRST ARRAY TEST STRUCTURE

The next stage of the project was development of complete readout circuitry for a simple array. The main goal of this task was to explore the issues related to development of readout for such set of detectors. These matters can be split into two main categories of electrical and layout ones, which will be discussed in the next part of the paper. The list of problems related to electrical design starts with the testing scenario. As it was stated previously, the single pixel readout circuit was intended for the in-lab tests using the signal generator as a replacement for detecting diode. Unfortunately, such solution cannot be used even in the case of very small array (in presented work 8x8 pixels) – on the one hand it is not possible to connect all inputs of charge amplifiers to the pads, and on the other hand – it is not practical to introduce any multiplexing for such small signals and high impedance nets. Due to these reasons it was decided to create the chip for manufacturing with SHIELD implantation process option, that means with detecting junctions below the BOX. In proposed solution entire readout circuit is built hierarchically, and the starting point is single pixel readout block, which consists of elements discussed in details in previous section: pixel diode polarization circuit, charge amplifier, shaper, peak detector, digital part (locking down functionality) and two current mirrors. Each row of the array contains 8 single-pixel readout circuits, together with digital multiplexer for MEAS_EN signal, analog multiplexer for peak detector output and current mirrors providing bias for each pixel. Finally, the array column consists of 8 complete rows, 8-to-1 analog multiplexer with output buffer for peak detector output signal, and current mirror.

A. The Most Important Components of Array Readout Circuit

As it was mentioned previously, the array test structure is intended to be manufactured in the full process option with detecting junctions, so some modification was necessary at the very beginning of pixel readout circuit. All detecting junctions share the n-type handling wafer as common cathode and their anodes (made of P-type SHIELD implantation below the BOX) are contacted using W-plugs with the charge amplifier located in device layer directly above the junction. The detecting junction anodes are kept at the voltage approx. 1.5V by a simple bias circuits, while common cathode will be biased with the high positive voltage (30-50V). The input of charge amplifiers are connected directly to detector anodes, this DC coupling and the feedback allows the circuit to operate with detector dark currents to 5-10nA. It is important in the case of radiation induced defects during exploitation of detectors. As another modification, a two-stage voltage amplifier was added to increase the sensitivity of charge amplifier (MEAS_EN is signaled for the input charge lower than 1000e). The next blocks within the circuitry – a peak detector, analog buffer and digital part are left unchanged in respect to the single pixel

readout circuit. In a single row of the array the MEAS_EN signals are grouped within the 8-bit long vector. Desired row is selected and connected to the output via eight 8-to-1 multiplexers controlled by 3 LSBs of address signal. This solution – parallel access to all sensors from chosen row enables the fast checking of particle presence via simple logical OR operation on each 8-bit word of MEAS_EN signals. When an excitation of detecting junction is signaled (corresponding bit in MEAS_EN vector is set), the analog signal from desired peak detector is fed to the output via two levels of analog multiplexers addressed by 3 bits (row) + 3 bits (column) address. The analog multiplexers are built in common 4-2-1 hierarchy but have non-typical internal architecture because of the split source topology of FETs in H035 process. In this topology the transistor source is permanently connected with body contact, that makes the drain and source not permutable. Hence, the typical transmission gate architecture based on two transistors cannot be used, because the substrate diodes will be forward biased for one direction of the signal. The more complicated structure with four transistors – two for each type connected in opposite direction is used instead. Hierarchical schematic of entire array is shown in Fig. 12.
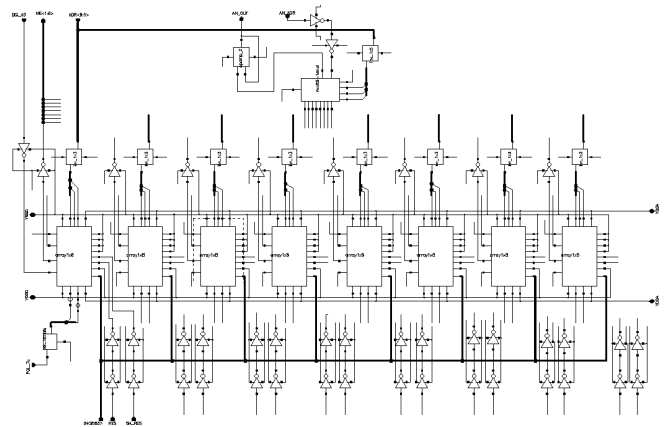

Fig. 12. Schematic of the readout circuit for 8x8 detector array.

Figure 13 presents test circuit used for simulation of entire array. The detecting junctions for all pixels were replaced with current sources generating square pulse of 10ns period, in parallel with 50fF capacitor. In Fig. 14 the simulation of diagonally stimulated array is presented: 8-bit long information vectors (MEAS_EN) are being read from subsequent columns. The high state of a bit within MEAS_EN vector informs, that corresponding detector cell (pixel) was stimulated by a particle. Hence, in diagonally stimulated array MEAS_EN vectors from subsequent columns contains "1" at subsequent bit positions corresponding to array rows. Complete operation of array readout – sending out the analog information from stimulated pixel is shown in Fig. 15. The energies of stimulating particles were chosen to cause alternately the 1000e and 8000e charge pulses in stimulated cells.

Another important issue was floorplanning and layout drawing for array test structure. As it was mentioned, charge amplifier cells have to be placed directly above detecting junctions to minimize the parasitics on interconnecting paths.
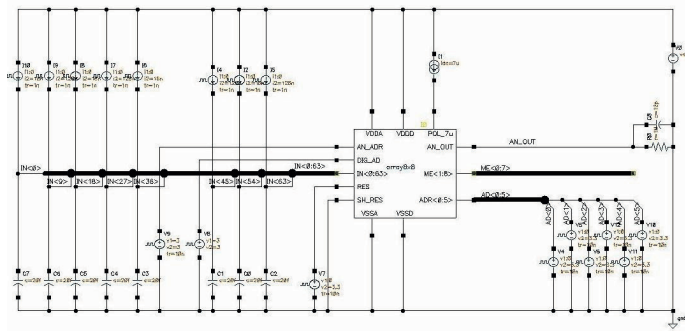
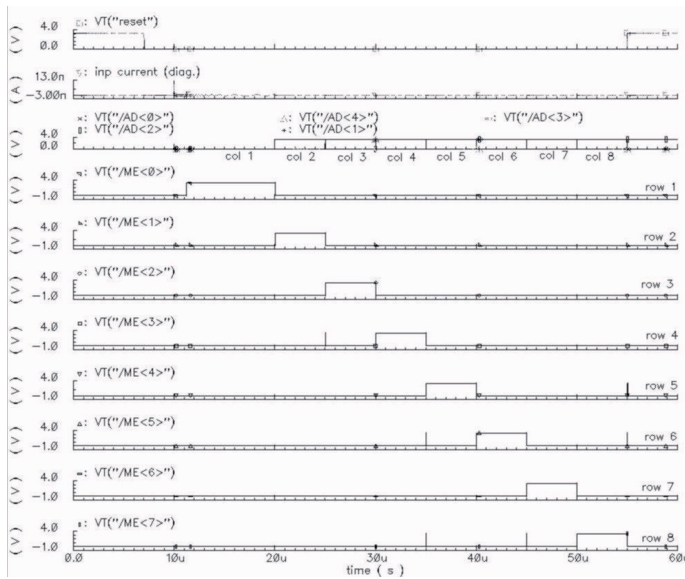Fig. 13. Schematic of testbench for 8x8 detector array.

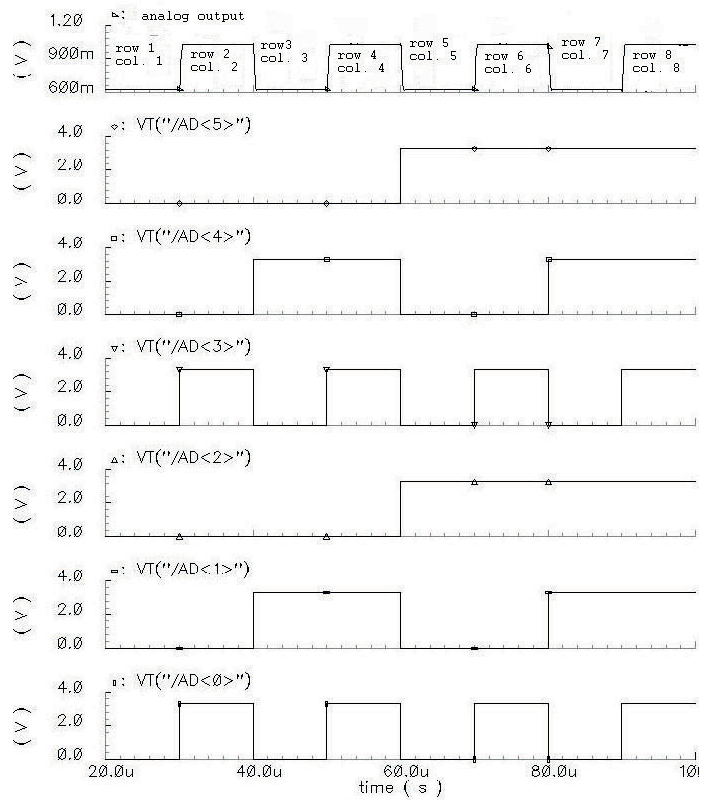Fig. 14. Simulation of readout operation for diagonally stimulated array.

Fig. 15. Simulation of readout operation from analog output of diagonally stimulated array.
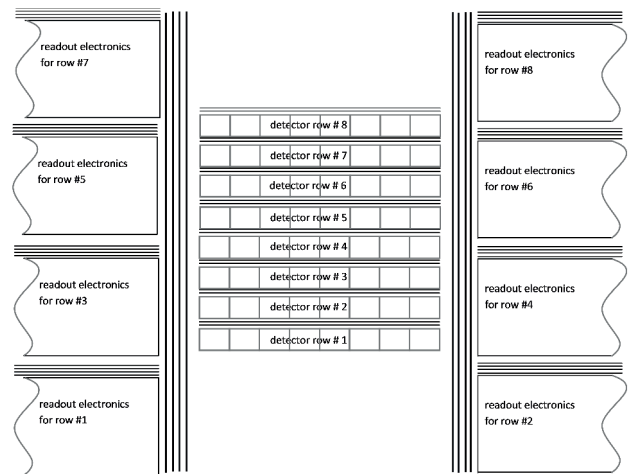
Fig. 16. Simplified view of detectors and readout block floorplan.

Hence the shape and area of charge amplifier is restricted to be as square as possible and have the linear dimensions close to 50um, which results in detector row (8 amplifiers above 8 junctions plus interconnections) of 560 x 60 mm dimensions. On the other hand, the readout electronics for one detector row (whole circuitry aside from charge amplifiers) has linear dimensions of 2018 x 410 mm. Such a misfit is known issue in integrating different types of detectors with redout electronics and requires special solutions to be used in layout. In described case it was decided to place the odd rows of readout electronics on the left side of detector array and the even rows on the right one, and to add vertical offset to detectors array. In this way the interconnection path length between charge amplifier and the rest of electronics were roughly balanced. Simplified view of proposed solution is presented in Fig. 16 .

The area separating detector array from the readout electronics at its left and right side was filled with vertical paths providing common signals for: two pairs of supply and ground, separate for analog and digital part, three LSBs of address, four MEAS_EN outputs, four analogue outputs, four bias current inputs and three control signals. Some components of the circuit, which are used as single instance, rather than a part of readout electronic rows are placed in the area below detectors

array. The most important among them are analog multiplexer and analog buffer (operational amplifier), digital buffers (set of inverters) and current mirror. The remaining empty area was filled with two large capacitors used for supply filtering. Due to relatively large layout dimensions resulting in long supply lines within the ring, additional ESD structures (supply voltage clamp) were distributed around the IC. Figure 17 presents layout of entire chip, while Fig. 18 shows some part of interconnection area to give the knowledge about its level of complication.
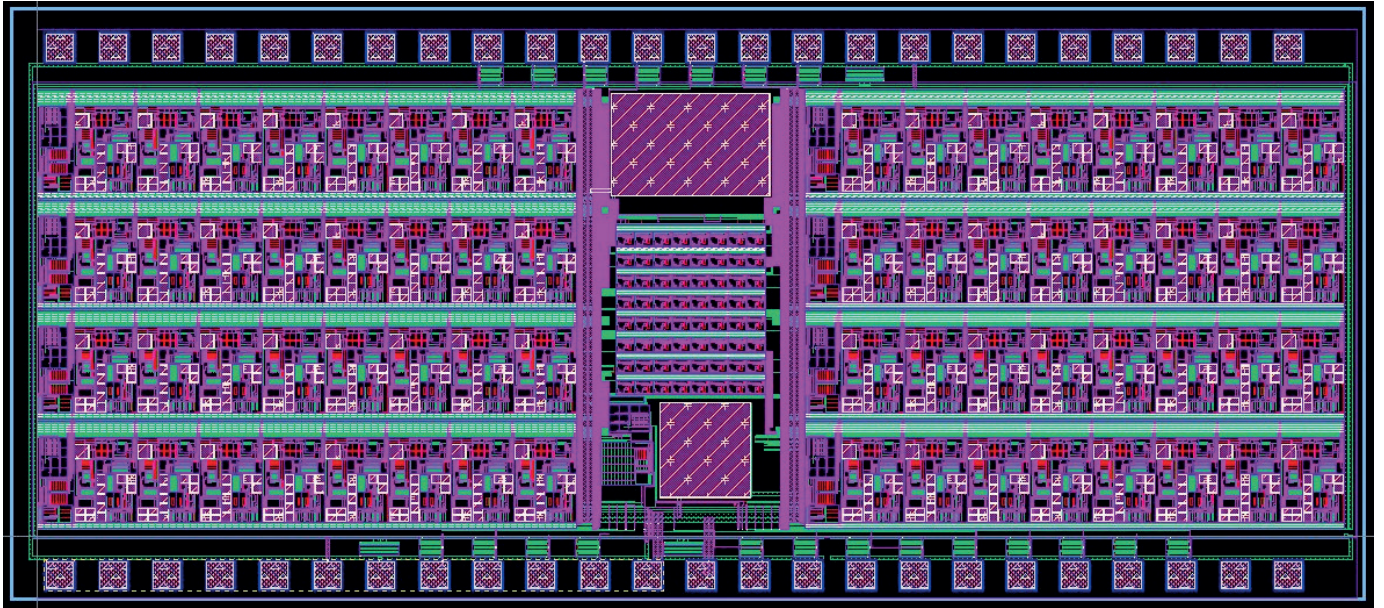
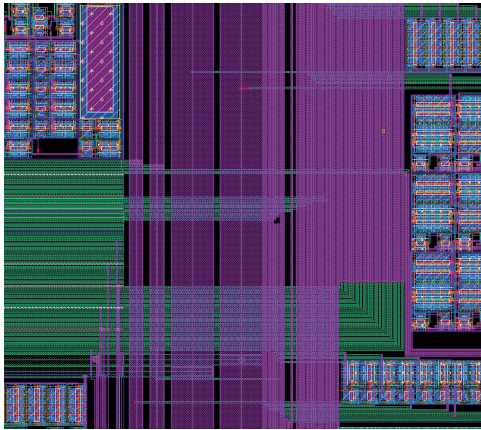Fig. 17. Layout of simple array readout teststructure.

Fig. 18. Layout detail – some part of interconnection area.

V. CONCLUSION

Two advanced readout circuits for read ionizing radiations detectors were developed basing on non-typical silicon process provided by IMS Duisburg. Measurements of manufactured test structure proved the concepts used in a circuit design, as well as the correctness of parts of layout verification procedures developed in ITE.

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