

### A family of high-power multilevel switched capacitor-based resonant DC-DC converters - operational parameters and novel concepts of topologies

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Abstract. This paper presents the concept of topologies and investigation results of switched-capacitor voltage multipliers designed for application in high power systems. The analyzed family of multilevel converters includes established topologies as well as novel concepts. The application of thyristors as well as the invention of novel concepts of multiplier topologies and appropriate control make it possible to achieve high efficiency, high voltage gain, reliable and simple DC-DC converters for high power systems. Based on analytical models of the SCVMs, the paper presents a discussion of the selection of components and the efficiency of the converters as a function of converted power as well as the voltage range on the input and the output side. The results are supported by computer simulations and demonstrative experimental tests.

Key words: DC-DC converter, high power converter, resonant converter, high voltage gain, zero-current switching.

#### 1. Introduction

The DC-DC voltage conversion is required in a huge number of applications; thus, a considerable progress in development of new topologies and systems of the DC-DC converters is presently observed. One of the crucial issues for DC-DC converters is increasing the voltage and power range which can be used, for instance, in such applications as DC grids interconnection, utilization of renewable energy power plants and DC loads. A high power converter should be characterized by high reliability and high efficiency; thus, the application of suitable switches as well as simple topology and control is a great advantage. The proposed topologies in the family of multilevel resonant switched capacitor voltage multipliers (SCVM) meet these requirements.

The application of the switched capacitor (SC) technology in power electronic converters has been addressed in scientific papers for years [1, 2]. However, a substantial development of the power converters supported by the SC technology is still observed. In the DC-DC conversion area, a number of topologies, concepts and families of the SC converters are proposed in [3–28]. For many high power applications, in kilowatt range, many new, attractive conversion methods based on SC converters are presented [3-16].

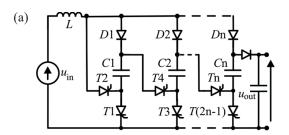
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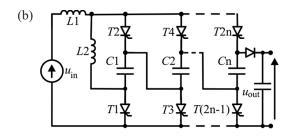
The SC converters operate using the principle of charge pumps and usually contain a large number of switches. However, high efficiency can be achieved in the SC converters by the application of resonant operation [4, 15]. The SC converters can also be designed in an efficient way thanks to an appropriate selection of passive and active components [4, 16]. The selection of the parameters of the passive components for an SCVM is a complex process and and it should be done considering the switch technology, power and required efficiency, which is demonstrated in [16].

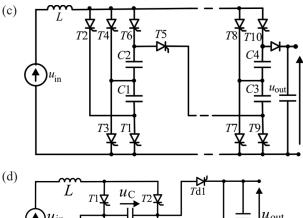
The SCVM topology is suitable for the application of thyristors as active switches [3, 4, 15]. Furthermore, the ability of bidirectional voltage blocking makes it possible to further optimize the SCVMs, as presented in [4, 26, 27], where the reduction of the number of switches is demonstrated in the topology called RSCVM. The application of thyristors creates possibilities for DC-DC conversion in resonant mode topology at high power, voltages and currents, owing to extremely high parameters of the thyristors. The resonant-mode operation is advantageous, because it makes turning-off the switches possible and assures zero current switching (ZCS) [4].

This paper, in Section 2, presents an analysis of the thyristor-based SCVM related to feasibility of the converter for high power application (Fig. 1a). The analytical results reach 500 kilowatts power, which makes it possible to demonstrate, in figures, the efficiency, range of currents as well as the value of LC parameters. Next, in Section 3, the thyristor-based topologies suitable for high power operation are presented (Figs. 1b, 1c, 1d). The evolution of the SCVM, presented in [4] is also

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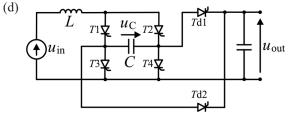


Fig. 1. The family of switched capacitor DC-DC converters analyzed in this paper: switched capacitor voltage multiplier (SCVM) [4] (a), switched capacitor voltage multiplier with reduced number of switches (RSCVM) [4, 26] (b), SCVM with higher frequency and reduced number of switches (HFRSCVM) [27] (c), voltage multiplier in full-bridge configuration (FBVM) (d)

analyzed here (Fig. 1b) with the original results of analysis reaching 500 kW of power. This Section also presents two novel topologies in the family of the high power DC-DC converters with the basic description of the operation principle and the assessment of prospective advantages.

## 2. Concept of operation and composition of the SCVM

The general concept of an SCVM converter is presented in Fig. 1. The topology makes it possible to boost the input voltage by charging the output capacitor by series connected switched capacitors and the input source. The switched capacitors are previously charged by a parallel connection to the source. A general description of the operation of the SCVMs can be found in [4, 15, 16].

The current and voltage of the capacitors during charging are

$$i_{\rm CI}(t) = \frac{U_{\rm in} - U_{\rm Cmin}}{\rho_{\rm I}} \sin \omega_{\rm I} t = I_{\rm Im} \sin \omega_{\rm I} t \tag{1}$$

$$u_{\rm CI}(t) = U_{\rm in} - (U_{\rm in} - U_{\rm Cmin})\cos\omega_{\rm I}t \tag{2}$$

$$\rho_{\rm I} = \sqrt{\frac{L}{nC}}, \qquad \omega_{\rm I} = \frac{1}{\sqrt{nLC}} \tag{3}$$

where:  $U_{\rm in}$  is the supply voltage, n is numbers of cells,  $U_{C \rm min}$  is the minimum voltage across capacitor C,  $r_{\rm I}$  is the characteristic impedance of the series LC circuit during charging,  $\omega_{\rm I}$  is the angular resonant frequency of the series LC circuit during charging.

Maximum capacitor voltage is for  $\omega_1 t = \pi$  (end of charging) and  $U_{\text{Cmin}} = 0$ :

$$U_{C\max} = 2U_{\rm in}.\tag{4}$$

Maximum capacitor current is equal to:

$$I_{\rm Cmax} = \frac{U_{\rm in}}{\rho_{\rm I}}.$$
 (5)

During discharging, the current and voltage of each capacitor are equal to:

$$i_{\rm CII}(t) = \frac{U_{\rm out} - U_{\rm in} - nU_{\rm Cmax}}{\rho_{\rm II}} \sin \omega_{\rm II} t = I_{\rm IIm} \sin \omega_{\rm II} t, \quad (6)$$

$$u_{\rm CII}(t) = \left(U_{\rm Cmax} - \frac{U_{\rm out} - U_{\rm in}}{n}\right) \cos\omega_{\rm II}t + \frac{U_{\rm out} - U_{\rm in}}{n}, \quad (7)$$

$$\rho_{\rm II} = \sqrt{\frac{nL}{C}}, \qquad \omega_{\rm II} = \sqrt{\frac{n}{LC}}$$
(8)

where:  $U_{\rm out}$  is the output voltage,  $U_{C\max}$  is the maximum voltage across capacitor C,  $\rho_{\rm II}$  is the characteristic impedance of the series LC circuit during discharging,  $\omega_{\rm II}$  is the angular resonant frequency of the series LC circuit during discharging.

From the above analysis, it follows that the converter has the following voltage gain and power:

$$U_{\text{out}} = (n+1)U_{\text{in}},\tag{9}$$

$$P = 2CU_{in}(U_{C_{max}} - U_{in})(n+1)f, \tag{10}$$

where f is the switching frequency equal to 1/T.

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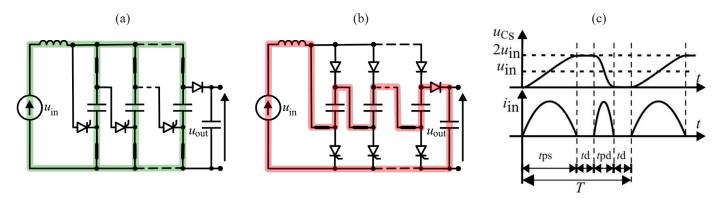


Fig. 2. The stages of charging and discharging of the switched capacitors of the SCVM (a), (b), and corresponding idealized waveforms of the switched capacitor voltage and the input current (c) with marked characteristic values and time points

Maximum power occurs for full recharging of the capacitors:

$$P_{\text{max}} = 2CfU_{\text{in}}^2(n+1) \tag{11}$$

Calculating efficiency should take into account power dissipation in the semiconductors, inductor and capacitors as well as the relation  $t_d/t_{ps}$  [4]:

$$\eta \approx 1 - \frac{\Delta U_{\rm T}(n+2) + n\Delta U_{\rm D}}{U_{\rm in}(n+1)} - \frac{\pi}{4} \sqrt{\frac{nC}{L}} \left( R_{\rm L} + \frac{R_{\rm C}}{n} \right)$$

$$\left( 1 + \frac{n}{n+1} \frac{2t_{\rm d}}{t_{\rm ps}} \right)$$

$$(12)$$

where:  $\Delta U_{\rm T}$  is the voltage drop across a thyristor,  $\Delta U_{\rm D}$  is the voltage drop across a diode,  $R_L$  is the resistance of the inductor,  $R_C$  is the resistance of a capacitor,  $t_{\rm ps}$  is the charging time,  $t_{\rm d}$  is the time required for turn-off of the thyristors (Fig. 2c).

The capacitance and inductance can be calculated based on maximum power  $P_{\rm max}$ , input voltage  $U_{\rm in}$ , number of cells n and times  $t_{\rm d}$  and  $t_{\rm ps}$  [4]:

$$C = \frac{P_{\text{max}}t_{\text{d}}}{nU_{\text{in}}^2} \left( \frac{t_{\text{ps}}}{t_{\text{d}}} + \frac{2n}{n+1} \right) \tag{13}$$

$$L = \frac{1}{nC} \left(\frac{t_{\rm ps}}{\pi}\right)^2 \tag{14}$$

#### 3. Feasibility of the high power SCVM

**3.1.** The concept of practical realization of a high power voltage multiplier. In a practical realization, an SCVM can be achieved with the use of commercially available switches. However, there can be significant differences in the realization between the low power low voltage converters and the high power and high voltage SCVMs. Low power SCVMs operating below 600 V on the output can be achieved as high frequency MOSFET-based converters. Such type of converters is analyzed in details in [15, 16], where the problems of selection of compo-

nents, feasibility, an impact of parasitic components as well as efficiency are presented. High power SCVMs as well as other switched capacitor converters need specific approach. One of the ideas presented in [4] is an implementation of thyristors for such a topology (Fig. 1a) to achieve benefits that follow from the voltage and current parameters of such switches, reliability, fault tolerant operation, simplicity of driver circuits. The high power solution of SCVMs has an input choke introduced as a part of resonant circuit (in contrary to the high frequency solution where the resonant circuit can utilize fragmented inductances achieved as air chokes and parasitic ones), and a converter in such a topology will be analyzed further. Fig. 3 presents experimental results, which confirm the feasibility of the SCVM in the thyristor technology.

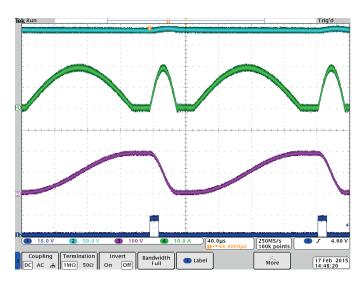


Fig. 3. The SCVM experimental results from 1kW model. Waveforms of the output voltage (2), input current (4), switched capacitor voltage (3) and control of the discharging thyristor (1)

**3.2. Voltage stresses on the semiconductor switches.** All the conventional switches as well as WBG-types can be used for SCVM converters. The selection of switches is determined by many aspects but one of the major ones is the voltage and cur-

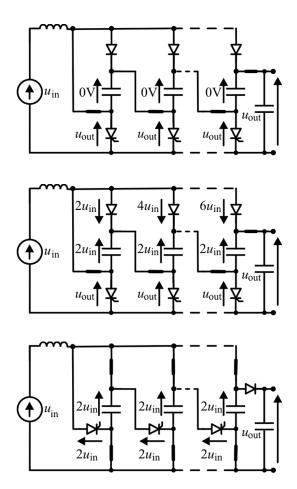


Fig. 4. The peak value of voltage stress in the ideal SCVM with the input choke

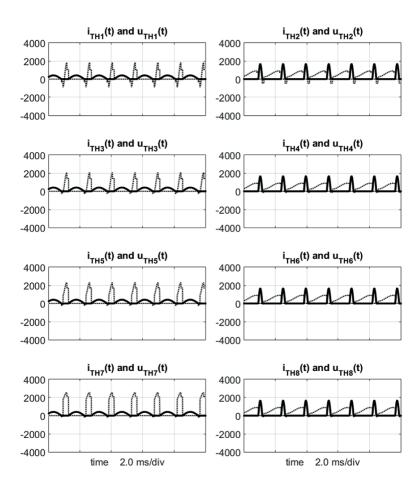


Fig. 5. Simulation results (Matlab/Simulink) of the operation of a 500 kW SCVM – waveforms of curents and voltages of the thyristors

rent stress. Fig. 4 presents voltage stresses in the ideal SCVM under the conditions where the voltage on the switches reaches the peak value. It is determined by the state of other switches and voltages on the switched capacitors. From the results presented in Fig. 5, it follows that the voltage distribution is not equal. The thyristors can experience a negative as well as a positive voltage stress in the off-state.

**3.3.** Current stresses on the switches in the SCVM. The current in the SCVM is shared between the switches during the charging stage; thus, it can be much lower than the input current:

$$I_{SAV} = \frac{P_{in}}{U_{in}(n+1)} \tag{15}$$

The thyristors in the discharging circuit have the same current value [4].

**3.4. Selection of suitable switches for the SCVM.** Suitable switch selection for a SCVM depends on the voltage ratio and power of the converter. MOSFET and SiC switches can be very attractive for lower voltage ratio of the converter (up to 600 V and 1700 V, respectively). For higher voltages, the converter can be configured with the use of thyristors. The thyristors have

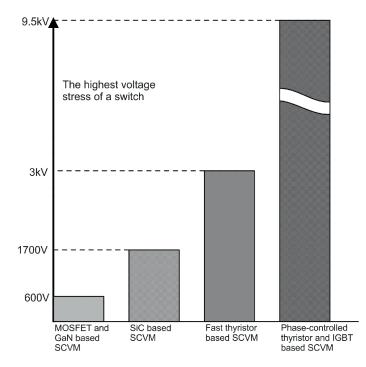


Fig. 6. Evaluation of the voltage range for switches for SCVM applications

good switching-off conditions in the SCVM due to ZCS operation. A problem can arise due to turn off-time, which causes that a specific delay between switching cycles is required.

Table 1 High power switches and evaluation for application in SCVM

Switch available on the market	Blocking voltage range [V] (approx.)	Range of current [A] (approx.)	Maximal output voltage of SCVM [V]	Factor affecting an additional delay between switching cycles	
SiC Mosfet	1700	1200	1700	_	
IGBT	6500	750	6500	Tail of current	
Fast thyristors	2000 (1200)	2100 (1500)	2000	Turn-off time (approx. 15–20 us) 80us	
Standard thyristors	7500	3500	9500	Turn-off time (approx. 0.1–1 ms)	

The turn-off delay of thyristors depends on the technology of the switch but approximately is in the range of (10–120) us. Owing to current sharing in the SCVM, the current stress of the switches is not a critical issue for their selection.

# 4. Thyristor-based high power SCVMs' operational parameters

**4.1. Switched capacitor and resonant choke selection.** The selection of components for the MOSFET-based SCVMs is analyzed in depth in [16]. The configuration of the thyristor-based SCVMs varies from that of the MOSFET-based converters, because the thyristor-based high power converters operate with lower frequency, require larger switched capacitors and discrete chokes (in contrary to PCB-type air chokes utilized in high frequency SCVMs).

The switched capacitors can be deeply discharged (to nearly zero voltage), which makes the converter optimized. Under such conditions, the relationship between the switched capacitors, operating frequency, inductance, power and parameters of switches becomes extremely important, e.g. (13, 14) and Fig. 7.

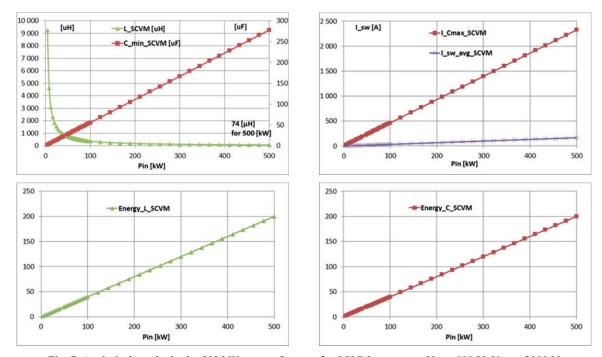


Fig. 7. Analytical results in the 500 kW range of power for SCVM converter.  $U_{\rm in} = 600$  V,  $U_{\rm out} = 3000$  V

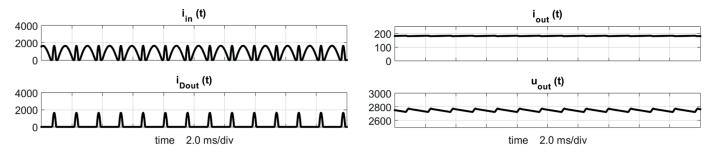


Fig. 8. Simulation results (Matlab/Simulink) of the operation of a 500 kW SCVM - waveforms of the input and output currents and voltage

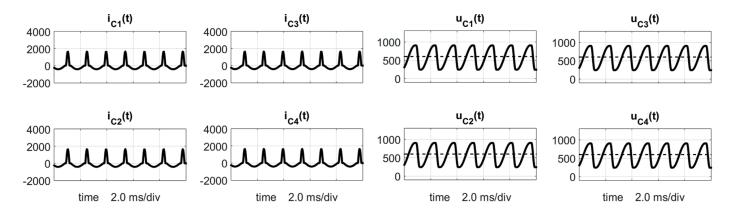


Fig. 9. Simulation results (Matlab/Simulink) of the operation of a 500 kW SCVM - current and voltage waveforms of the switched capacitors

**4.2. Efficiency of the thyristor-based SCVM.** In [4], an efficiency vs. power for the 1 kW SCVM it presented. However, the efficiency is a function of many parameters such as resistances, input voltage, forward voltages of switches and diodes, as well as the dead-time, which is demonstrated in Fig. 10 in the range of 500 kW according to (12). The last parameter, namely the dead time, has a very important impact on the efficiency.

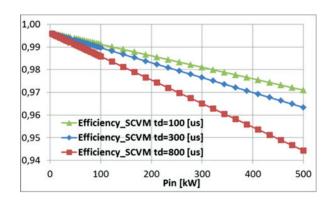


Fig. 10. Analytical results in the 500 kW range of power for SCVM converter.  $U_{\rm in}=600$  V,  $U_{\rm out}=3000$  V, n=4, variables  $t_{\rm d}=100\div800$  [µs] and inductance  $L_{\rm SCVM}={\rm const}$ 

# 5. Evolution of the topology concepts in high power DC-DC SC-based systems

# **5.1. SCVM** with a reduced number of switches (RSCVM). Figure 11 presents the concept of the thyristor-based SCVM with a reduced number of switches (RSCVM) [4]. The major advantage of the RSCVM is an operation without switches in the discharging branches. However, the lower recharging frequency of the switched capacitors, lower frequency of the output capacitor charging, as well as lower efficiency are its disadvantage. Figure 11 to Fig. 16 present results related to the operation of the RSCVM: analytical ones (Fig. 11), simulations (Figs. 12–15), and experimental tests based on a 1 kW model (Fig. 16).

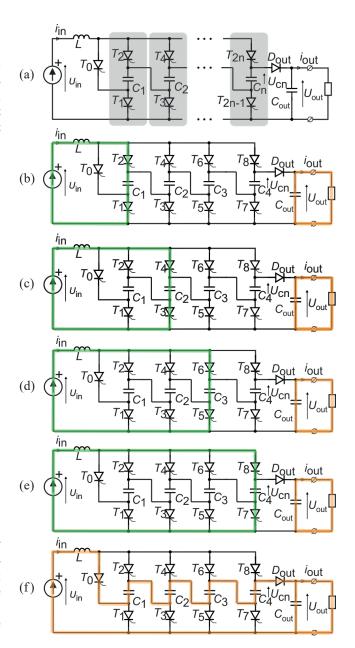


Fig. 11. The thyristor-based four-cell SCVM with reduced number of switches (RSCVM) [4, 26]

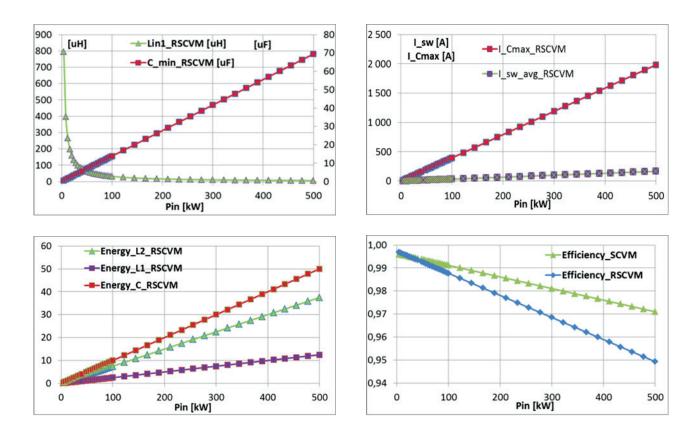


Fig. 12. Analytical results in the 500 kW range of power for RSCVM converter.  $U_{\rm in} = 600$  V,  $U_{\rm out} = 3000$  V

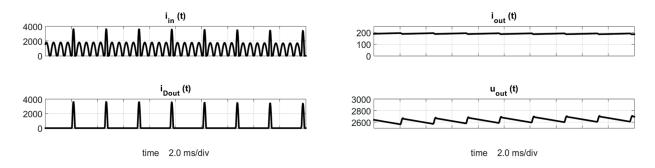


Fig. 13. Simulation results (Matlab/Simulink) of the operation of a 500 kW RSCVM - waveforms of the input and output currents and voltage

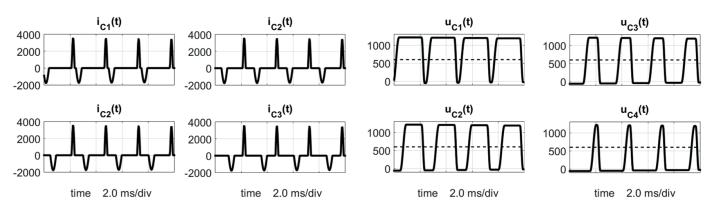


Fig. 14. Simulation results (Matlab/Simulink) of the operation of a 500 kW RSCVM - current and voltage waveforms of the switched capacitors

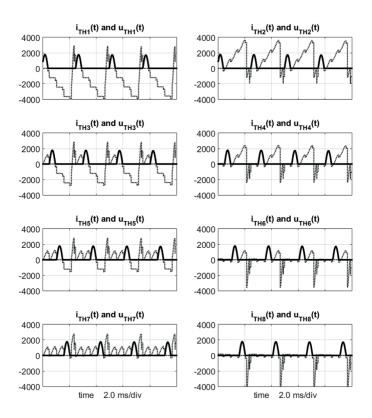


Fig. 15. Simulation results (Matlab/Simulink) of the operation of a 500 kW RSCVM – waveforms of curents and voltages of the thyristors

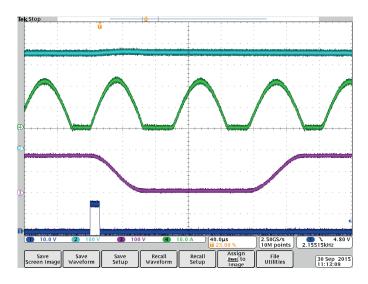


Fig. 16. The RSCVM experimental results from 1kW model. Waveforms of the output voltage (2), input current (4), switched capacitor voltage (3) and control of the discharging thyristor (1)

# **5.2.** The concept of the thyristor-based SCVM with higher frequency and reduced number of switches (HFRSCVM). Figure 17 presents the concept of the thyristor-based SCVM with higher frequency and reduced number of switches (HFRSCVM) [27], which represents a compromise between the SCVM and RSCVM. In comparison to the RSCVM, the converter is able to achieve the charging cycle in many cells simultaneously. Thus,

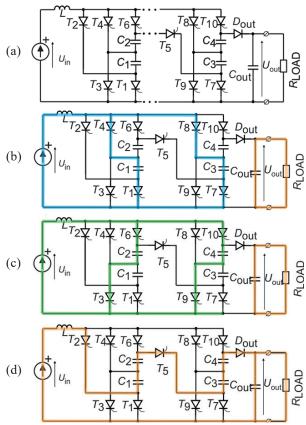


Fig. 17. The thyristor-based four-cell SCVM with reduced number of switches and increased switching frequency (HFRSCVM) [26]

the converter has bigger frequency of operation, which makes it possible to limit the current stresses and volume of passive components. Figures 18–20 present simulation results where the particular waveforms of power components are demonstrated.

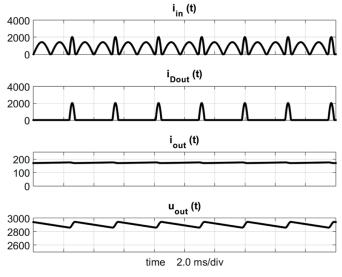


Fig. 18. Simulation results (Matlab/Simulink) of the operation of a  $500~\mathrm{kW}$  HFRSCVM – waveforms of input and output currents and voltage

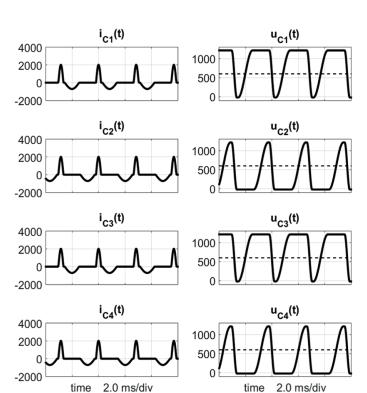


Fig. 19. Simulation results (Matlab/Simulink) of the operation of a 500 kW HFRSCVM – current and voltage waveforms of the switched capacitors

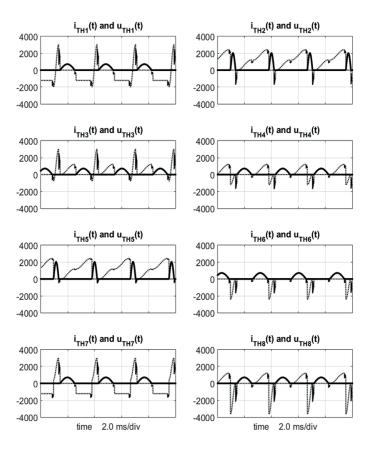


Fig. 20. Simulation results (Matlab/Simulink) of the operation of a 500 kW HFRSCVM - waveforms of curents and voltages of the thyristors  $\,$ 

**5.3.** The concept of the thyristor-based voltage multiplier in full-bridge configuration. The thyristor-based voltage multiplier in the full-bridge configuration (Fig. 21a) operates in two modes. In mode I, the switched capacitor C is being charged using n current pulses (Figs. 21b, 21c, 23, 24). In mode II (Fig. 21d for odd n, and Figs. 21d and 21e consecutively – for even n) the output capacitor is being charged and a part (or all) of the energy stored in capacitor C is transferred to the output capacitor  $C_{\text{out}}$ .

Basic equations for steady-state operation, valid for initial voltage across capacitor C in the range of  $0 \le U_{01} \le U_{in}$ , are presented below. It has been assumed that the power electronic switches and the other components of the converter are ideal, and the input  $(U_{in})$  and output  $(U_{out})$  voltages are constant.

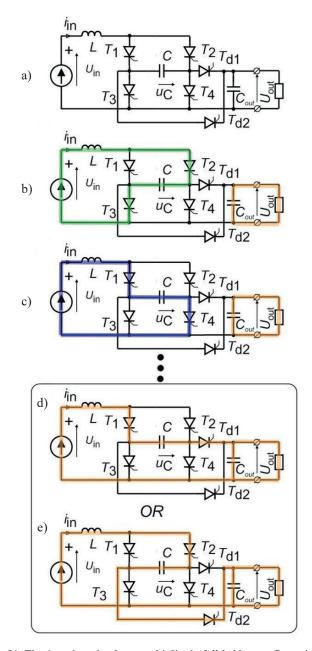


Fig. 21. Thyristor-based voltage multiplier in full-bridge configuration (FBVM) – circuit diagram and current paths

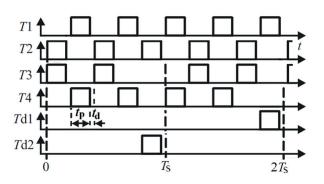


Fig. 22. Conduction times of thyristors in the converter for n = 4

The conduction times of the thyristors for n = 4 are shown in Fig. 22.  $T_{\rm S}$  (16) is the switching cycle, comprising n pulses of charging the switched capacitor C and one pulse charging the output capacitor  $C_{\rm out}$ , and

$$T_{\rm S} = 1/f_{\rm S} = (n+1)(t_{\rm p} + t_{\rm d}); \ t_{\rm p} = \pi \sqrt{LC}; \ t_{\rm d} \ge t_{\rm q} \ (16)$$

where  $t_p$  is the duration of each current pulse,  $t_d$  is the time necessary for turn-off of the thyristors;  $t_q$  is the turn-off time of the thyristors (a physical parameter of a device).

For n = 4, the thyristor conduction sequence is  $[(T_2T_3, T_1T_4), (T_2T_3, T_1T_4), T_2T_{d2}], [(T_1T_4, T_2T_3), (T_1T_4, T_2T_3), T_1T_{d1}].$  This sequence, in which the conduction order of the thyristors is different in two consecutive cycles (Fig. 22), is necessary for even n, to ensure the same direction of the initial condition  $U_{01}$  of the voltage across capacitor C with regard to the input voltage at the beginning of each cycle. However, in the case of odd n, the conduction order of the thyristors is the same in each switching cycle  $T_S$ .

The amplitude of the last current pulse n in mode I is

$$I_{\text{pnm}} = |I_{Cnm}| = \frac{(2n-1)U_{in} - U_{01}}{\rho}$$
 (17)

where  $I_{\rm pnm}$  is the amplitude of the current through the thyristors,  $I_{\rm Cnm}$  is the amplitude of the switched capacitor current,  $U_{01}$  is the initial condition of voltage across C at the beginning of each cycle, and  $\rho = \sqrt{L/C}$  is the characteristic impedance of the LC circuit.

The amplitude of the current pulse charging the output capacitor (mode II) is given by

$$I_{Coutnm} = \frac{nU_{\rm in} - U_{01}}{\rho} \tag{18}$$

The output voltage is

$$U_{\text{out}} = (n+1)U_{\text{in}}.$$
 (19)

Maximum voltage across capacitor C equals

$$U_{Cm} = 2nU_{in} - U_{01} (20)$$

with its highest value at  $U_{01} = 0$  expressed by

$$U_{C\max} = 2nU_{\text{in}}. (21)$$

Power of the inverter is equal to

$$P = \frac{2C}{T_C} U_{\text{in}} (nU_{\text{in}} - U_{01}) =$$

$$= 2(n+1) C f_S U_{\text{in}} (nU_{\text{in}} - U_{01}).$$
(22)

Maximum power occurs at  $U_{01} = 0$ 

$$P_{\text{max}} = \frac{2nC}{T_C} U_{\text{in}}^2 = 2n(n+1)Cf_S U_{\text{in}}^2.$$
 (23)

For set values of n,  $U_{in}$ , C,  $f_{S}$  and P, the initial condition can be calculated from (22)

$$U_{01} = nU_{\rm in} - \frac{P}{2(n+1)Cf_SU_{\rm in}}.$$
 (24)

The converter can operate correctly at a constant frequency in the way described above for

$$0 \le U_{01} \le U_{\rm in}. \tag{25}$$

For  $U_{01}=0$  (largest load), capacitor C reaches maximum voltage (21) and then fully discharges transferring all the energy to  $C_{\rm out}$ . Therefore, the power in this case is maximum. Simulated waveforms for this case are shown in Fig. 23. The value of capacitance C in the simulation has been chosen higher than that calculated theoretically, to obtain the assumed power

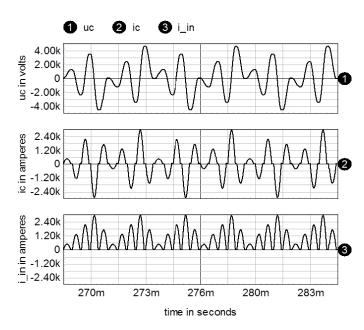


Fig. 23. Waveforms in thyristor-based voltage multiplier – maximum power,  $U_{01}\approx 0$  V,  $P_{\text{out\_max}}=498$  kW,  $U_{\text{out}}=2.82$  kV, 1-voltage across capacitor C, 2-capacitor C current, 3-input current.  $U_{\text{in}}=600$  V, n=4, L=205  $\mu\text{H}$ , C=110  $\mu\text{F}$ . ICAP/4 simulation results

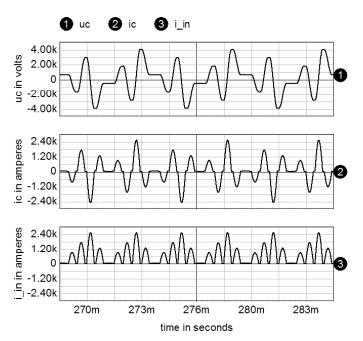


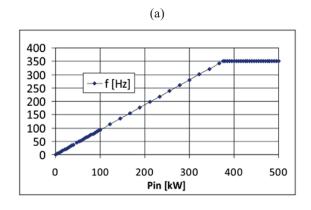
Fig. 24. Waveforms in thyristor-based voltage multiplier – minimum power,  $U_{01}=U_{\rm in}, P_{\rm out\_min}=376$  kW,  $U_{\rm out}=2.90$  kV. 1-voltage across capacitor C, 2-capacitor C current, 3-input current.  $U_{\rm in}=600$  V, n=4, L=205  $\mu H$ , C=110  $\mu F$ . ICAP/4 simulation results

of 500 kW under consideration of voltage drops in the circuit. The inductance has been decreased accordingly, to maintain the constant duration  $t_p$  of each current pulse.

For  $U_{01} = U_{\rm in}$  (lightest permissible load – Fig. 24) there is no current in the first time interval  $t_{\rm p} + t_{\rm d}$  (compare Fig. 23 and Fig. 24) and the capacitor charges finally to voltage  $U_{\rm Cm} = (2n-1)U_{\rm in}$  (20), which is lower than that in the previous case with  $U_{01} = 0$ . This operating point determines the converter's minimum power and critical load at a fixed frequency  $f_{\rm S}$ .

Substitution of (24) into (25) yields

$$2(n-1)(n+1)Cf_SU_{in}^2 \le P \le 2n(n+1)Cf_SU_{in}^2$$
. (26)



Hence

$$P_{\min} = \frac{n-1}{n} P_{\max}.$$
 (27)

For example, in the case of  $P_{\text{max}} = 500 \text{ kW}$ ,  $P_{\text{min}}$  equals 375 kW for n = 4 and only 450 kW for n = 10. Therefore, at a fixed switching frequency  $f_{\text{S}}$ , the range of the converter's output power is narrow, especially for high n.

In the case of resistive load,  $P_{\min}$  occurs at critical load

$$R_{\text{out\_crit}} = \frac{n+1}{2(n-1)Cf_S}.$$
 (28)

For  $R_{\rm out} > R_{\rm out\_crit}$ , the initial voltage  $U_{01} > U_{\rm in}$ . The output voltage and power are given by

$$U_{\text{out}} = nU_{\text{in}} + U_{01}$$
 (29)

$$P = 2(n-1)Cf_S U_{\rm in}(nU_{\rm in} + U_{01})$$
 (30)

and they are both higher than those at  $R_{\text{out}} \leq R_{\text{out crit.}}$ 

To conclude, at fixed values of n,  $U_{\rm in}$ , C and  $f_{\rm S}$ , the converter cannot operate with power less than  $P_{\rm min}$  given by (27). A simple way to control power in a wide range is variation of frequency  $f_{\rm S}$  to obtain  $P < P_{\rm min}$  (27), e. g., by appropriate increasing time  $t_{\rm d}$ , so as to maintain  $U_{01} = U_{\rm in}$ . Substitution of  $U_{01} = U_{\rm in}$  into (22) yields

$$P = 2(n-1)(n+1)Cf_SU_{\rm in}^2.$$
 (31)

Therefore, the converter power is proportional to the switching frequency  $f_S$ .

Figures 25 and 26 show some parameters of the converter as a function of input power  $P_{\rm in}$  in the range from 0 to  $P_{\rm max}$ . At lower power,  $U_{01}=U_{\rm in}$ , and  $U_{C\rm m}$ , the current amplitudes and the efficiency stay constant. At higher powers, switching frequency stays constant, and  $U_{C\rm m}$  and the current amplitudes increase with rising power, and the efficiency slightly decreases.

Another possibility of power control can be using a special control system. Based on the measurements of the switched

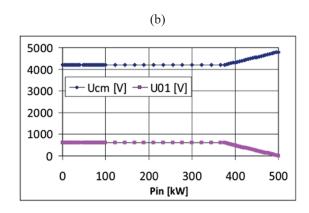
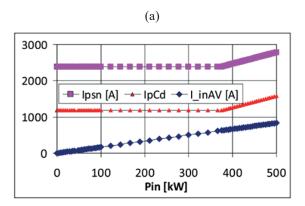


Fig. 25. Switching frequency  $f_S$  (a), initial voltage  $U_{01}$  and peak voltage  $U_{Cm}$  across capacitor C (b) as a function of input power  $P_{in}$ .  $U_{in} = 600$  V, n = 4,  $L = 227 \mu H$ ,  $C = 99.2 \mu F$ 



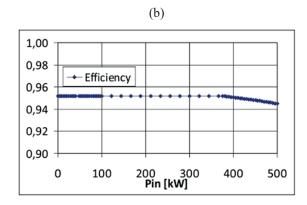


Fig. 26. Mean value of input current  $I_{\text{inAV}}$ , peak value of current  $I_{\text{psn}}$  charging capacitor C and peak value of current  $I_{\text{pCd}}$  charging the output capacitor (a) and converter's efficiency (b) as a function of input power  $P_{\text{in}}$ .  $U_{\text{in}} = 600 \text{ V}$ , n = 4,  $L = 227 \mu\text{H}$ ,  $C = 99.2 \mu\text{F}$ 

capacitor and the output capacitor voltages, it will determine the required number of pulses n and the times of firing the thyristors. Moreover, the system can be designed to control the converter's output voltage in a wide range. These tasks are intended to be addressed in future research.

#### 6. Conclusions

The family of switched capacitor high power converters is presented and analyzed in the paper. All the converters operate in the ZCS mode; thus, they can achieve high efficiency. From the comparison it follows that the switched capacitor voltage multiplier can operate with high power, high voltage and high currents by the application of thyristors as active switches. Results demonstrating the selection of passive components as well as efficiency and stresses on the switches show that the converter is feasible as a high power converter.

The paper presents also some optimized topologies of the SCVM demonstrating the differences in concept of operation and design requirements in relation to the SCVM. The presented results show that optimizing the converter towards the reduction of the number of switches affects the operational parameters and sizing of the passive components. The application of

Table. 2. Comparison of selected parameters of discussed converters

The characteristic	SCVM	R SCVM	HFR SCVM	FBVM
Number of switches and diodes	8/5	8/1	10/1	6/0
Efficiency	High	High	High	High
Ripple of the output voltage	Lower	Higher	Medium	Higher
Maximum voltage stresses on switches	$U_{ m out}$	$U_{ m out}$	$U_{ m out}$	$U_{ m out}$

thyristor technology makes it possible to create other, original topologies of the DC-DC converters, which is demonstrated based on FBVM converter. The presented analysis and results show that the converter assures high voltage gain under the high power conversion capability. A suitable, but not complicated, control is necessary in this case.

The paper shows the differences between the topologies, which can be a basis for the selection of the converter for a particular application. From the presented content, it also follows that the converters need further research on topologies, control, practical realization and implementation.

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