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A low-voltage CMOS negative impedance converter for analogue filtering applications

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Abstract. A novel current-inversion type negative impedance converter (CNIC) is presented. It is built without the use of any resistors. Furthermore, a second-order low-pass filter based on this CNIC is also analysed. It shows a bandwidth of 50 MHz at 320 μW power consumption and 2 V supply voltage when realized in a 0.35 μm CMOS process.

Key words: CMOS, negative impedance converter, continuous-time filters.

1. Introduction

Low-voltage high-frequency continuous-time filters are still required in many applications and are the subject of continuing research [1–5]. There are many techniques to realize integrated filters, including OTA-C, Opamp-RC and MOSFET-C-Opamp. The latter two show high dynamic range at low supply voltage, but their frequency operating range is usually limited to several megahertz. Transconductance filters are dedicated to higher frequencies. However, the design of a low-distortion low-voltage OTA is still challenging. Taking this into account, it is worth to revise the obsolete concept of active RC-filter synthesis based on a current-inversion negative impedance converter (CNIC) as an active element [6–9].

NIC filters show higher sensitivity to their component values than popular LC-ladder type realizations [10]. Furthermore, traditional NICs containing resistors are not precise enough for accurate filter characteristics. A CMOS converter proposed in this paper does not include any resistors and shows a very well controlled conversion factor k. Our Monte Carlo simulation results of the filter prove that exact frequency characteristics can be maintained even at low supply voltage when the proposed converter is applied.

2. NIC – principle of operation

2.1. Large-signal properties. A circuit diagram of the new CNIC is shown in Fig. 1a. All transistors operate in the saturation region and have their bodies connected to ground or power supply, depending on the transistor type. Please take a notice that M1 and M2 can also work in the triode region. Dimensions of the devices are related by $(\mathrm{W/L})_2 = k(\mathrm{W/L})_1$ and $(\mathrm{W/L})_4 = k(\mathrm{W/L})_3$, and the corresponding bias currents by $I_{B2} = kI_{B1}$, where k is a positive real number. For simplicity of analysis, we assume that the current sources M5 and M6 are ideal.

The voltages and currents of an ideal CNIC are related by [11]:

$$v_1 = v_2 \tag{1a}$$

$$i_1 = (1/k)i_2 \tag{1b}$$

Using the standard square-law model for MOS devices, the main large-signal voltage relationship of the circuit from Fig. 1a takes an implicit form:

$$v_1 = v_2 + v_{GS4} - v_{GS3} \cong v_2 + \Delta V_T\,(v_1, v_2) \tag{2}$$

where $\Delta V_T = V_{T4} - V_{T3}$. As Eq. (2) indicates, the major source of distortion of the above-mentioned relationship comes from the difference between threshold voltages of M3 and M4. Since v_1 is nearly equal to v_2, the body effect of M3 and M4 has very weak influence on ΔV_T. The major source of difference between V_{T4} and V_{T3} is the DBIL (drain-induced barrier lowering) effect of M3 since v_{DS3} swings considerably more than v_{DS4}. For $k1$, M3 and M4 have different dimensions and their narrow-channel effect could cause ΔV_T to be significantly larger. To minimize this effect the layouts of M3 and M4 should be built out of the equal size unity devices.

Next, the currents i_1 and i_2 can be expressed as:

$$i_1 = i_{D1} - I_{B1} = K_1\left(v_{GS1} - V_{T1}\right)^2\left(1 + \lambda\left(v_1 - V_{SS}\right)\right) - I_{B1} \tag{3a}$$

$$i_2 = i_{D2} - I_{B2} = K_2\left(v_{GS2} - V_{T2}\right)^2\left(1 + \lambda\left(v_2 - V_{SS}\right)\right) - I_{B2} \tag{3b}$$

where $K_i = 0.5\mu_0 \mathrm{C_{OX}}(\mathrm{W/L})_\mathrm{i}$ and λ is the channel-length modulation index. Taking into account that $v_{gs1} = v_{gs2}$, $K_2 = kK_1$ and $I_{B2} = kI_{B1}$, and assuming $V_{T1} = V_{T2}$, rearrangement of (3a) and (3b) leads to:

$$i_1 = \frac{1}{k} i_2 \frac{1 - \lambda V_{SS} + \lambda v_1}{1 - \lambda V_{SS} + \lambda v_2} + I_{B1}\left(\frac{1 - \lambda V_{SS} + \lambda v_1}{1 - \lambda V_{SS} + \lambda v_2} - 1\right) \tag{4}$$

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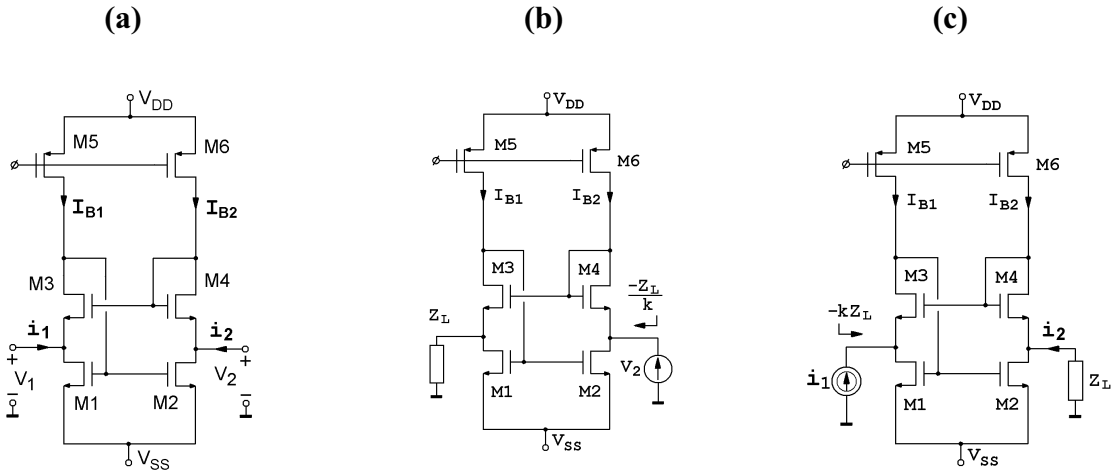

Fig. 1. Current-inversion type negative impedance converter (CNIC), a) circuit diagram, b) configuration for voltage excitation, c) configuration for current excitation

Comparison between (1b) and (4) shows that the accuracy of the current transfer is affected by the previously defined inaccurate voltage transfer. It can also be seen from (4) that the simultaneous increase of a channel length for M1 and M2 leads to a lower error of the current transfer function.

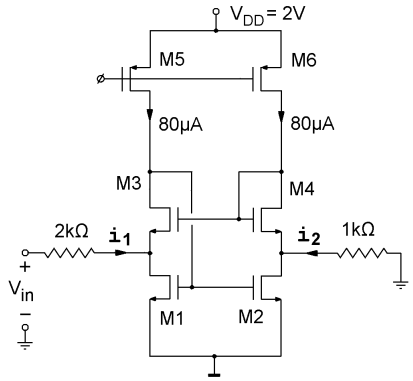

Fig. 2. Circuit configuration for the k test

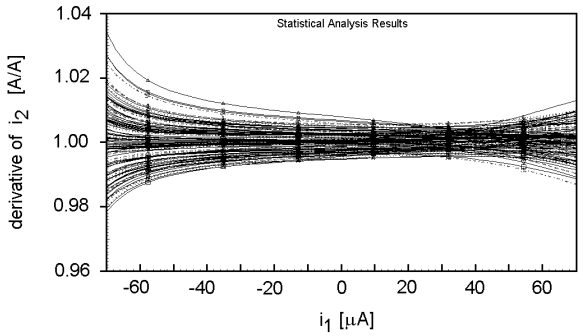

Fig. 3. Monte Carlo analysis of the CNIC from Fig. 2

The proposed CNIC is designed for $k = 1$ and for an input current range of $\pm 60\mu$A at a single supply voltage $V_{DD} = 2$ V. Dimensions for both transistor are as follows: $(W/L)_1 = (W/L)_2 = 20\mu m/2\mu m$, $(W/L)_3 = (W/L)_4 = 20\mu m/1\mu m$. I_{B1} and I_{B2} are chosen to be equal to 80 μA. The conversion factor k was tested in a circuit configuration shown in Fig. 2, where the small-signal ground was set to 0.4 V. The results of a 100-sweep Monte Carlo analysis shown in Figs. 2, 3 indicate that k is kept within $0.98 \div 1.02$ A/A. Such a good control of k is practically unfeasible with traditional converters containing linear resistors because the transistor match is considerably better than the corresponding match among polysilicon resistors in a typical CMOS process [12]. The simulations were performed using Cadence Spectre solver. A 0.35 μm CMOS process from AMS was chosen for this design. A standard deviation for the normal distribution of both V_T and K were assumed as $\sigma(\Delta V_T) = 10^{-2}(WL)^{-0.5}$ and $\sigma(\Delta K/K) = 2 \cdot 10^{-3}(WL)^{-0.5}$, respectively, according to the Pelgrom model [13] and the appropriate process parameters.

2.2. Small-signal properties. The proposed CNIC contains two feedback loops: a local high-gain negative feedback loop (M1 and M3) and a global low-gain positive feedback loop. The CNIC from Fig. 1a is stable when the V_2 terminal is loaded with low impedance (or short-circuited) and is unstable when the same node is loaded with high impedance (or opened). Therefore, two dedicated configurations for both voltage and current excitations should be distinguished. They are shown in Figs. 1b and 1c, respectively. In order to estimate the number of poles and zeros in the $i_2(s)/i_1(s)$ transmittance, a small-signal equivalent model of the circuit from Fig. 1c was built and the corresponding symbolic transfer function was derived with the aid of MATHEMATICA. The presence of two feedback loops makes this transfer function very complex in the high-frequency range and the following simplifications had to be assumed: $g_{dsi} = 0$, $C_{gdi} = 0$ and $C_{dbi} = C_{sbi} = C_d$ for $i = 1, \ldots, 6$. Moreover, k was assumed to be equal to 1, so $g_{m1} = g_{m2} = g_{m1,2}$, $g_{m3} = g_{m4} = g_{m3,4}$ and $g_{mb3} = g_{mb4} = g_{mb}$. For all above-stated assumptions, a simplified small-signal transfer function of the loaded CNIC (Fig. 1c) was obtained:

$$\frac{i_2(s)}{i_1(s)} = g_L \frac{a_3 s^3 + a_2 s^2 + a_1 s + a_0}{b_4 s^4 + b_3 s^3 + b_2 s^2 + b_1 s + b_0} \tag{5}$$

where coefficients a_i and b_i are given by (6a) and (6b), respectively.

$$\begin{aligned}
a_0 &= g_{m12} g_{m34} (g_{mb} + g_{m34}) \\
a_1 &= g_{m1,2} \left[2g_{mb}(C_d + C_{gs3,4}) + g_{m3,4}(2C_d + C_{gs3,4}) \right] \\
a_2 &= -2C_{gs3,4} g_{m3,4} (C_d + C_{gs1,2}) \\
a_3 &= -2C_{gs3,4}^2 (C_d + C_{gs1,2})
\end{aligned} \tag{6a}$$

$$\begin{aligned}
b_0 &= g_L g_{m1,2} g_{M3,4} (g_{mb} + g_{m3,4}) \\
b_1 &= 2(C_d + C_{gs3,4})(g_{mB} + g_L) g_{mb} g_{m1,2} \\
&\quad + 2(C_d + C_{gs1,2})(g_{mb} + g_{m3,4}) g_L g_{m3,4} \\
&\quad + (2C_d + C_{gs3,4})(2g_{mb} + g_L) g_{m1,2} g_{m3,4} \\
&\quad + 2C_d g_{m1,2} g_{m3,4}^2 \\
b_2 &= 2\left[C_d + C_{gs1,2} \right] \cdot \left[(2C_d + C_{gs3,4})(g_{mb}^2 + 2g_{m3,4} g_L) \right. \\
&\quad + 2g_{mb} g_L (C_d + C_{gs3,4}) + g_{mb} g_{m3,4} (C_{gs3,4} + 6C_d) \\
&\quad \left. + 4g_{m3,4}^2 C_d \right] \\
&\quad + 2g_{m1,2}(2C_d + C_{gs3,4})(g_{mb} C_d + g_{mb} C_{gs3,4} + g_{m3,4} C_d) \\
b_3 &= 8C_d^2 (2g_{mb} + g_L + 3g_{m3,4})(C_d + C_{gs1,2}) \\
&\quad + 4C_d C_{gs3,4}(5g_{mb} + 3g_L + 5g_{m3,4})(C_d + C_{gs1,2}) \\
&\quad + 2C_{gs3,4}^2 (g_{mb} + g_L)(C_d + C_{gs1,2}) \\
b_4 &= 4(C_d + C_{gs1,2})(4C_d^3 + 8C_d^2 C_{gs3,4} + 3C_d C_{gs3,4}^2)
\end{aligned} \tag{6b}$$

Table 1
Pole-zero locations of CNIC obtained by Eq. (4) and HSPICE analysis

	$g_L = 0.1$ mS		$g_L = 1$ mS	
p(pole) z(zero)	from Eq. (4)	HSPICE	from Eq. (4)	HSPICE
p [MHz]	−213−j83	−175−j78	−254	−258
p [MHz]	−213+j83	−175+j78	−735−j203	−579−j271
p [MHz]	−794	−679	−735+j203	−579+j271
p [MHz]	−1276	−1139	−3645	−2708
z [MHz]	−452	−466	−452	−465
z [MHz]	587	566	587	565
z [MHz]	−1372	−1516	−1372	−1516

It can be noticed from (5) that the transfer function has 3 zeros and 4 poles. Furthermore, the locations of all zeros do not depend on g_L (6a). The small-signal parameters in (6a) and (6b) were obtained from simulations and they are as follows: C_d = 12 fF, $C_{gs1,2}$ = 140 fF, $C_{gs3,4}$ = 69 fF, $g_{m1,2}$ = 375 μS, $g_{m3,4}$ = 535 μS, g_{mb} = 120 μS. Next, the poles and zeros of the converter transfer function were numerically calculated with MATHEMATICA from Eq. (5). They were also obtained directly from the pole-zero analysis performed with HSPICE. The results summarized in Table 1 show good agreement between the theoretical predictions and the simulations, specifically for the locations of all zeros and of the dominant pole. The simulations also confirmed that there are no more than 3 zeros and 4 poles in the transfer function, and the frequency location of all zeros do not depend on the value of a resistive load. The simulated amplitude response is flat and a −3-dB frequency is above 100 MHz, as shown in Fig. 4. If it is not the case, the existing peaks can be damped by increasing the total capacitance seen at the drain of M3 device. According to Table 1, the phase response reaches −270 degrees at high frequencies due to 4 poles in LHP, 2 zeros in LHP and 1 zero in RHP.

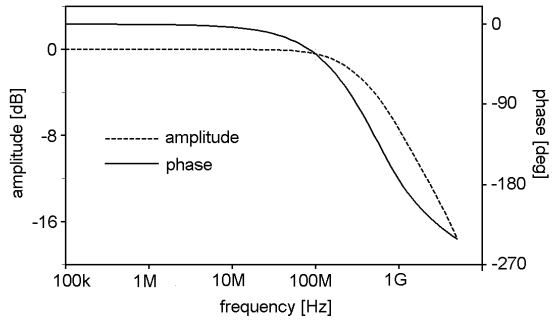

Fig. 4. Small-signal current responses of the converter from Fig. 1c

3. Second-order filter

In order to show the application of the proposed converter, a simple low-pass filter was designed as shown in Fig. 5 [4,7]. The input voltage V_{in} is applied with respect to a small-signal ground equal to 0.4 V. The dimensions of the transistor are as follows: (W/L)$_1$ = (W/L)$_2$ = 20μm/2μm, (W/L)$_3$ = (W/L)$_4$ = 20μm/1μm, (W/L)$_3$ = (W/L)$_4$ = 100μm/2μm. The arrangement of passive components guarantees that the converter is always stable. Furthermore, both capacitors are grounded. Thus, parasitic capacitances associated with their top plates can be taken into account by a simple modification of the nominal capacitances. Assuming the ideal converter, the transfer function of the considered filter from Fig. 5 can be expressed in the well-known form:

$$\frac{V_{out}}{V_{in}} = \frac{\omega_0^2}{s^2 + s\omega_0/Q + \omega_0^2} \tag{7}$$

where the pulsation ω_0 and the quality factor Q are given as follow:

$$\omega_0 = \frac{1}{RC\sqrt{\alpha\beta}}, \quad Q = \frac{\sqrt{\alpha\beta}}{\alpha\beta - k\beta + 1} \tag{8}$$

and coefficients α, β are defined in the Fig. 5 Eq. (8) indicates that ω_0 can be tuned by adjusting R or C without disturbing Q. Both resistors and capacitors in Fig. 5 can be built as an array of unite elements when realized in an integrated circuit technology. Thus, the ω_0 tuning can be realized by a digital control of the resistor or capacitor values, preserving their ratio at the same time. An arbitrary Chebyshev-approximation filter prototype was chosen to be implemented for demonstration purposes only. Its tabulated coefficients α, β and the

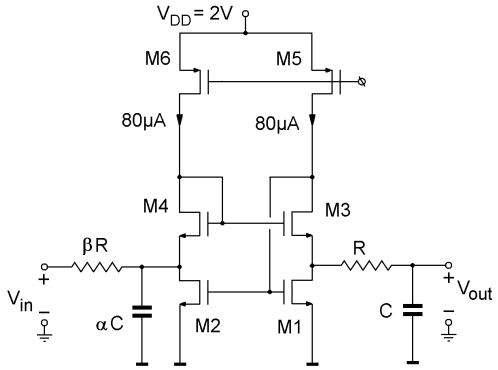

Fig. 5. Second-order low-pass Chebyshev filter with 1 dB passband ripple ($\alpha = 1.05$, $\beta = 0.95$)

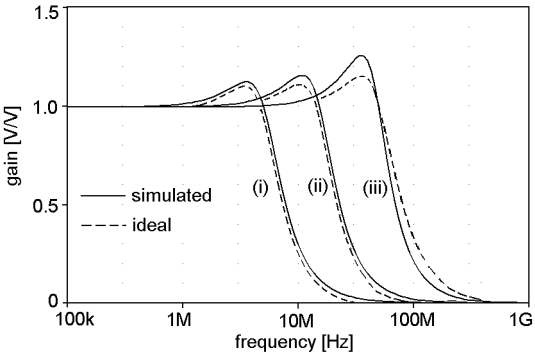

Fig. 6. AC response family of the filter from Fig. 5
(i) R = 1 kΩ, C = 30 pF, passband = 5.1 MHz
(ii) R = 1 kΩ, C = 10 pF, passband = 15.3 MHz
(iii) R = 1 kΩ, C = 3 pF, passband = 49.6 MHz

conversion factor k are 1.047, 0.954 and 1, respectively [8]. The filter was layouted and resimulated including all extracted parasitics. Taking the technology resolution into account, α and β were chosen to be equal to 1.05 and 0.95, respectively. R was assumed to be 1 kΩ and both resistors were realized using a high-resistive polysilicon. An AC response of the filter was simulated for 3 different C: 3 pF, 10 pF and 30 pF (Fig. 6). The simulated curves exhibit very good agreement with the ideal ones. However, for higher frequencies the passband ripples become larger due to the frequency limitations of the CNIC. A 500 sweep Monte Carlo analysis in respect to the parameters of active devices was performed for the case $C = 10$ pF (Fig. 7). A linear scale was chosen for the ordinate axis in Fig. 7 to emphasize a very small variation in the simulated AC response due to the transistor mismatch. The simulated THD of the filter is 1% for a 1 MHz 0.56V$_{textrmpp}$ input sine signal (case $C = 10$ pF). The equivalent input noise integrated in the passband is 39 μV$_{\mathrm{RMS}}$, what gives the signal-to-noise ratio 73 dB. For the case $C = 3$ pF, THD is 1% for 10 MHz 0.36 Vpp input signal, the equivalent input noise is 67 μV$_{\mathrm{RMS}}$, what gives the signal-to-noise ratio 65 dB. The filter consumes 320 μW power from 2 V single supply. Some other advanced simulations have not indicated any filter instability.

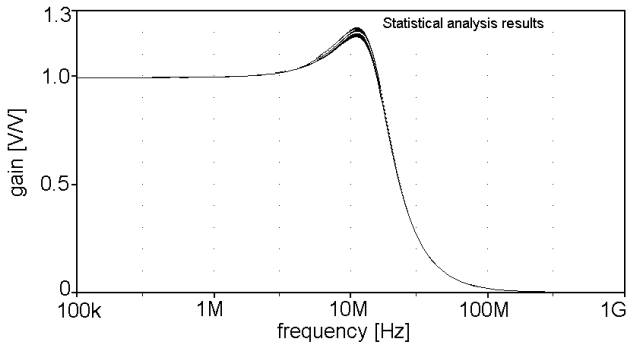

Fig. 7. Monte Carlo analysis (500 sweeps) of the filter from Fig. 5

4. Conclusions

Nowadays, continuous-time analogue filters are dominated by the Opamp-RC and OTA-C topologies based on the LC-ladder prototypes. Although, CNIC-RC filters show higher sensitivity to the values of elements, the presented simulation results show that it is possible to achieve accurate filter characteristics. A simple second-order CNIC section shows wideband characteristics and can be used for various types of low-voltage low-power prefilters in the front-end of a mobile receiver. A higher-order filter can be obtained by cascading the second-order sections as shown in Fig. 8, where all building blocks are similar. An input voltage V_{in} is separated by the buffer (M1, M2, M3) and each filter section is separated by the shifter/buffer block (M10÷M15). The parasitic input capacitance of the shifter/buffer can be simply included into a capacitor C_1 of the preceding filter section.

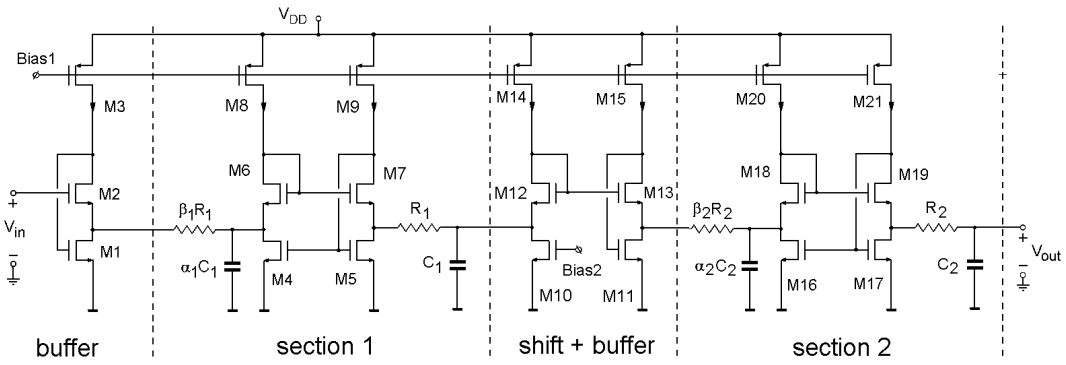

Fig. 8. Fourth-order filter

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