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Design of efficient multiplier with low power and high-speed using PTL (Pass Transistor Logic)

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***Abstract*—The demand for low-power, high-speed, and area efficient digital circuits has driven the exploration of alternative logic families such as Pass Transistor Logic (PTL). The design of a multiplier circuit that leverages the inherent advantages of PTL to achieve significant improvements in power consumption, operational speed and silicon area usage. The proposed multiplier using PTL-based logic gates to generate partial products, followed by a reduction tree and a final addition stage, all optimized for performance and efficiency. Key design challenges, such as voltage degradation and level restoration inherent in PTL circuits, is addressed through carefully designed voltage restoration techniques and custom PTL cells. The architecture is compared against conventional CMOS-based multipliers to demonstrate its superiority in terms of power efficiency and speed. All the circuits are simulated using ECAD tools to analyze the power, delay, area and Power-Delay-Product (PDP) of the multiplier to highlight a substantial reduction in power consumption and a faster operation, making the PTL-based multiplier an ideal circuit for high-performance and low-power applications in modern digital systems. The proposed work contributes to the field of low-power digital design by showcasing the potential of PTL in creating multipliers which are not only efficient but also scalable for future technology nodes.**

***Keywords*—Low power; Full adder; Multiplier; Delay; Pass Transistor**

I. INTRODUCTION

IN this new world of digital technology, electronic systems have taken up an integral position in several activities that govern life today. Core parts include microprocessors, digital communication modules, and signal processing units that provide the back bone of such systems. Scaling has brought several issues; chief among these is the consumption of power and constraints imposed by the area on the silicon that further deter its viability and extensive application. With the rapid advancement of emerging technologies such as the Internet of Things (IoT), smart homes, and intelligent urban infrastructure, the demand for energy-efficient and compact circuit designs has become more pressing than ever. It is crucial to achieve a balance between reduced power consumption, minimized chip area, and high computational efficiency in the design of modern digital circuits. Arithmetic circuits, which include adders, multipliers, and dividers, are the basic building blocks of many digital applications. Of these, multipliers are the most important since their efficiency determines the overall computational speed and power consumption of a system. Thus, optimizing multiplier topologies and developing creative computation methodologies are critical for obtaining extremely fast, low-energy multiplication, which improves the functionality of electronic devices in real-world applications. In this research, we offer a power-aware a maximum of eight-bit multiplier that uses Pass Transistor Logic (PTL) to operate at fast rates while taking up little space. It uses the Modified Booth Encoding (MBE) technique to improve speed and minimize both the power dissipated and the circuit complexity. With these optimizations, the proposed multiplier has achieved substantial improvements in speed and energy efficiency and so is highly suited for modern digital applications.

II. BACKGROUND

Multipliers play a crucial role in various computational applications, making them a significant area of research [2] [3]. Over the years, researchers have proposed various approaches to improve multiplier efficiency using different algorithms, including array multipliers, carry-save architectures, Wallace tree structures, and optimized Booth encoding techniques [4] [5]. These design strategies aim at an optimal balance be- tween power consumption, processing speed, and silicon area. Modern multiplier architectures have become increasingly sophisticated, but further performance enhancements require the development of novel standard cells and circuit optimization techniques. Traditionally, standard cell designs are based on Complementary Metal-Oxide-Semiconductor. However, in order to improve circuit functionality even more, experts have focused on Pass Transistor Logic (PTL) [6]. For example, in [6], all electronics circuits computing-in-memory macro was reported, whereby both CMOS-based and PTL-based complete adders were integrated in the adder tree, increasing computational efficiency by 30% In [7], a PTL-based full adder was also integrated into an RCA circuit to reduce the transistor count. Furthermore, In [8], a PTL-based Booth selection circuit incorporated a 54×54 multiplier lowered transistor usage by 45%, demonstrating the potential of PTL in arithmetic circuits.

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Despite these advantages, PTL-based designs present certain challenges. While they require fewer transistors, this does not always equate to a smaller layout area due to their intricate connectivity, which can lower layout utilization [9]. Furthermore, cascading PTL circuits cause large delays, as observed in [10]. In order to minimize this problem, researchers in [11] placed inverters at the output of PTL circuits, which doubled the power and area. The hybrid approach of [9] alternated PTL and CMOS full adders, effectively reducing cascading delay while remaining efficient. Moreover, PTL circuits often de- grade with threshold voltage and have poor driving capability. Therefore, some design modifications are needed. In [9],for example, inverters were placed after every two PTL units to improve logic restoration and reliability. However, with these trade-offs, the successful implementation of PTL in arithmetic circuits requires careful design considerations to maximize performance while minimizing associated drawbacks.

III. PROPOSED DESIGN

In this study, we present a maximum of eight-bit multiplier that uses Pass Transistor Logic (PTL) circuits to optimize the 3 main portions of the multiplier. The circuits has been carried out in a 45nm technology node with enhanced performance on the grounds of power, area, and speed.

TABLE I
A COMPARATIVE EVALUATION OF CMOS AND PTL DESIGNS IN 45NM TECHNOLOGY WITH 0.9V VOLTAGE SUPPLY AT 500 MHZ

Design	Transistor Count	Power(µW)	Delay(ps)	Area(µm2)
CMOS-XOR	12	17.16	65.0	0.78
PTL-XOR	6	0.389	34.20	0.39
CMOS-HA	20	6.929	87.72	1.47
PTL-HA	12	1.964	87.71	0.88
CMOS-FA	28	2.505	147.0	1.67
PTL-FA	16	11.06	43.39	1.47

A. Design and Evaluation of PTL-Basin 45nm Technology

Figure 1(a), Figure 1(b), Figure 1(c) illustrate the PTL architectures for fundamental logic gates, including the XOR gate, half adder (HA), and full adder (FA), [11], [12]. To critically assess the advantages of the use of PTL instead of traditional CMOS-based implementations, we designed the standard cells for these units based on the 45 nm process design rules with a 7-track architecture. Simulations were performed at an operating voltage of 0.9V and a frequency of 500MHz, and the performance was compared against equivalent CMOS-based standard cells. The comparative analysis is summarized in Table I. The results indicate that while the PTL-based full adder (FA) achieves reductions in area and power consumption, it exhibits a slightly higher critical path delay than its CMOS counterpart. This implies that although PTL FA contributes to energy and area efficiency, its impact on the overall circuit speed needs to be carefully considered in high-performance applications. On the other hand, PTL-based XOR and HA structures show remarkable improvements in power efficiency, delay reduction, and area minimization compared to CMOS equivalents. An important aspect of practical implementations is the driving capability of PTL circuits. Because of their inherent design, PTL-based structures often have limited load-driving capacity.

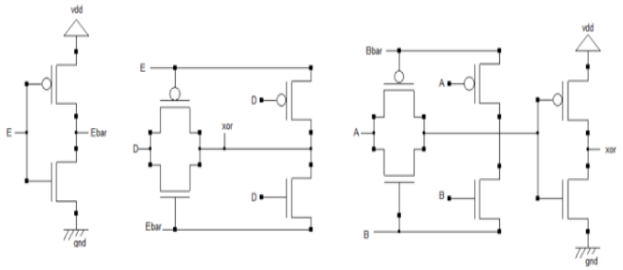

Fig. 1(a) 6/8-T PTL-XOR

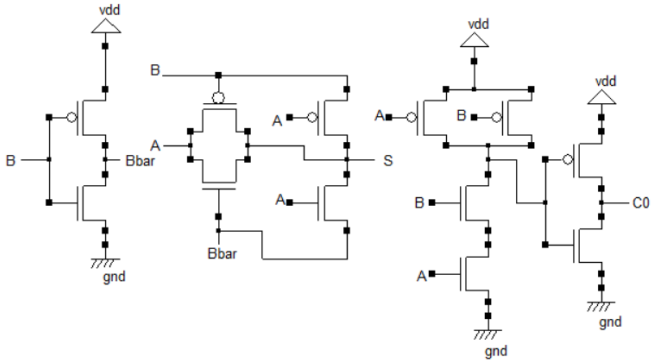

Fig. 1(b) PTL-HA

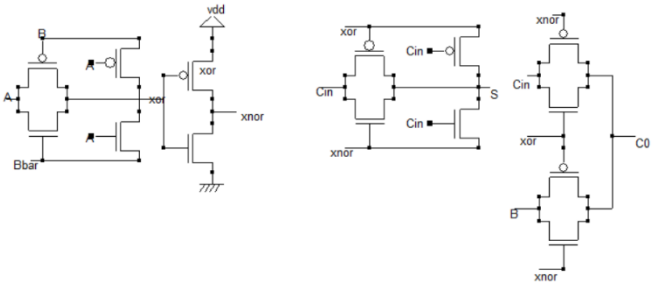

Fig. 1(c) PTL-FA

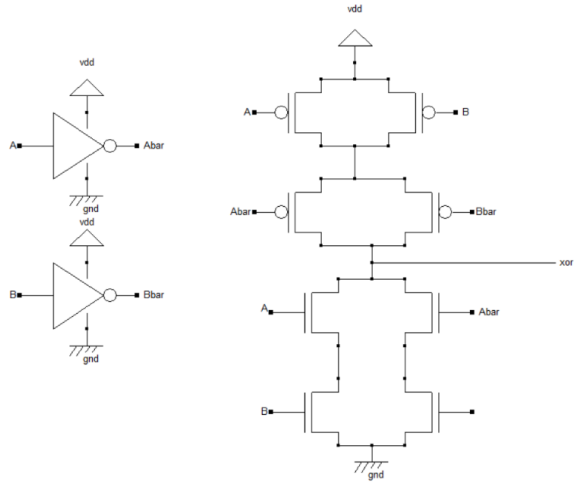

Fig. 2(a) CMOS-XOR

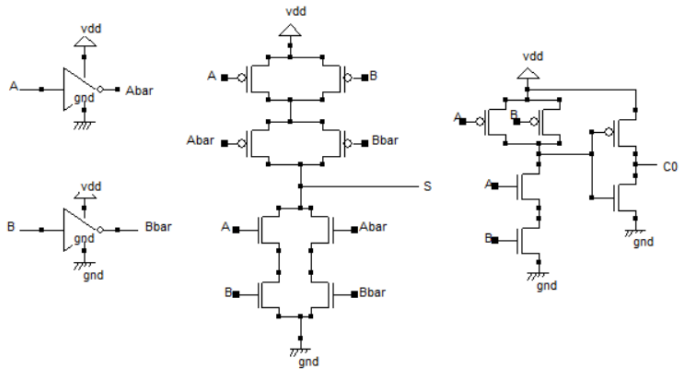

Fig. 2(b) CMOS-HA

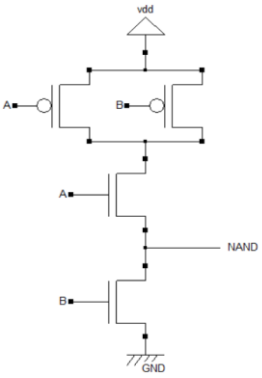

Fig. 4(a) CMOS-NAND

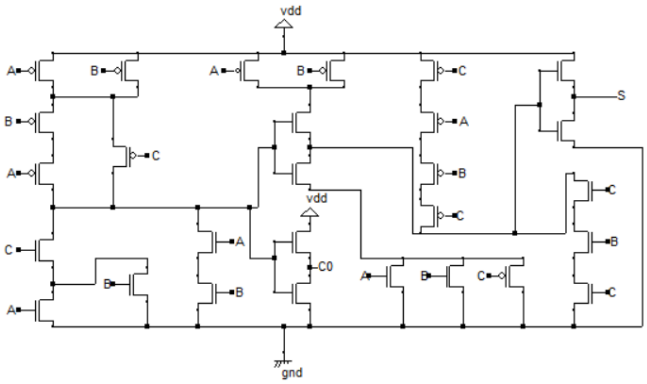

Fig. 2(c) CMOS-FA

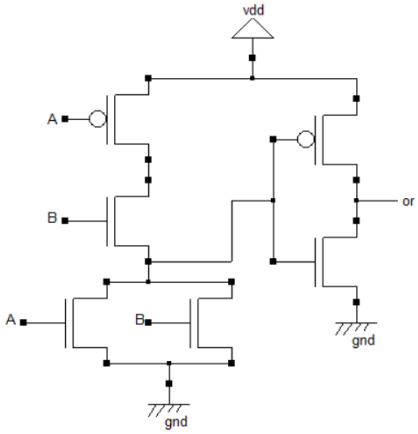

Fig.4 (b) CMOS-OR

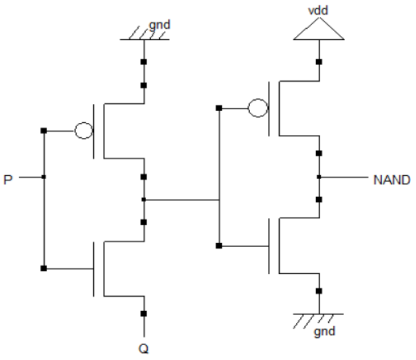

Fig. 3(a) PTL-NAND

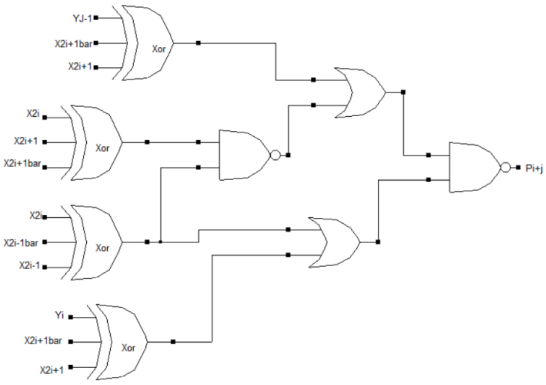

Fig. 5(a) PTL-MBE

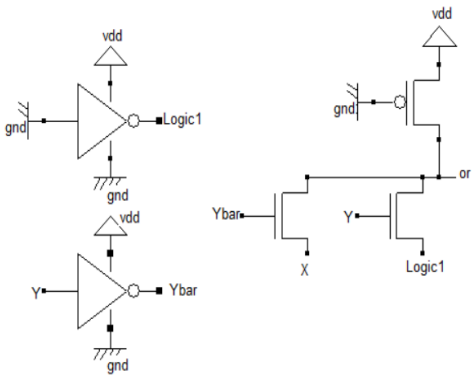

Fig. 3(b) PTL-OR

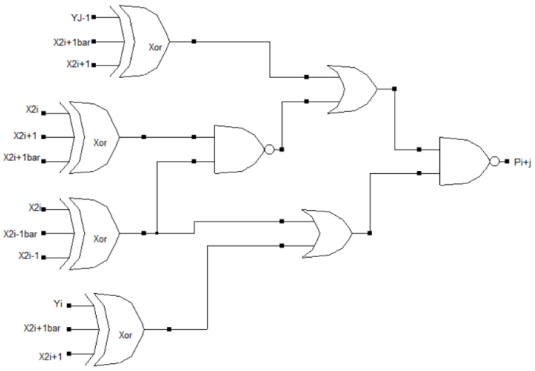

Fig. 5(b) CMOS-MBE

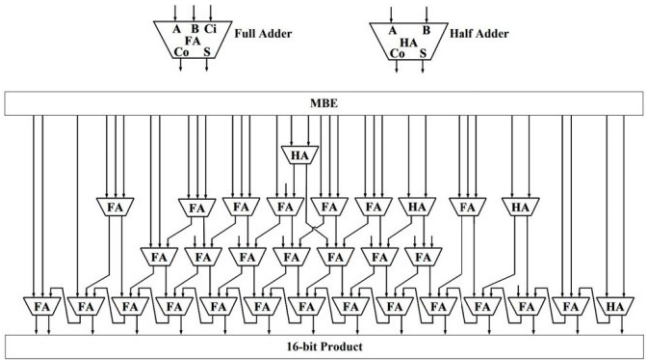

Fig. 6. Synthesized Multiplier using CMOS logic

To increase signal integrity and circuit stability, design adjustments such as integrating inverters at the output can be employed, as seen in the 8T XOR gate in Figure 1(a).

B. *Using PTL-Based Cells*

The Modified Booth Encoder(MBE), in Figure. 5(a), mainly depends on the XOR gate. Integration of the PTL-based XOR gates into the MBE requires incorporating buffers for the X2i+1 and X2i-1 to make sure that B and Bbar are generated correctly. Such encoding for Booth multiplication relies on such signals, buffered globally to retain signal integrity with the associated minimal overhead in the total transistor count. In the vast majority of situations, a performance level as obtained from a 6T XOR gate will suffice, while for a need for additional drive strength a 6T XOR gate as described below in Figure. 1(a)- is advantageous. This arrangement includes a full-swing PTL_XNOR gate constructed Using an inverter for increased driving strength. The usage of PTL_XOR gates in the Booth encoder significantly decreases the multiplier's circuit surface area and power consumption. As shown in Figure 6, the multiplier is synthesized using half adders (HA) and full adders (FA). The use of PTL-based HA significantly minimizes the energy consumption and latency in the multiplier design. Though the integration of PTL FA further lowers circuit power, this could increase the critical path delay a little bit. Although the maximum delay of PTL

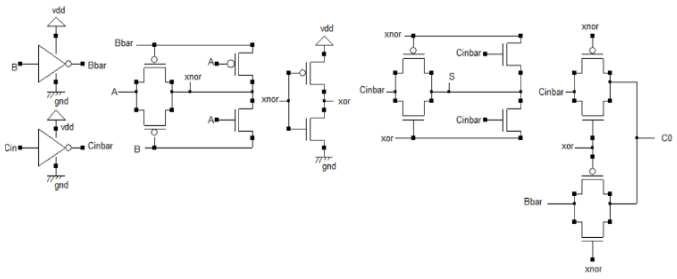

Fig. 7. PTL_FAinv

FA is longer than CMOS, the PTL_FA involves lower carry propagation delay. This is the characteristic that makes PTL_FA a suitable candidate for improving the overall efficiency of the multiplier circuit. To make it more efficient in terms of its circuitry, we present PTL-based FA with Inversion (FAinv) in Fig. 7. The major difference between the PTL_FA and FAinv is the type of carry input (Cin) and carry output (Co) structure used. For example, compared to the PTL_FA circuit that uses simple carry signals, FAinv features an inverted carry input and output to achieve a better propagation of the signals. The corresponding Boolean equations of their functions are: For the PTL_FA:

$$S = A \oplus B \oplus Cin \quad (i)$$
$$Co = (A \odot B) \cdot B + (A \oplus B) \cdot Cin \quad (ii)$$

For the proposed FAinv:

$$S = A \oplus B \oplus Cinbar \quad (iii)$$
$$Co = (A \odot B) \cdot Bbar + (A \oplus B) \cdot Cinbar \quad (iv)$$

These basic arithmetic blocks implementation via PTL-based logic significantly improve power efficiency and reduce the required area, which definitely motivates the idea of using this for the design of low-power and high-speed-multipliers.

C. *Proposed PTL-Based Multiplier*

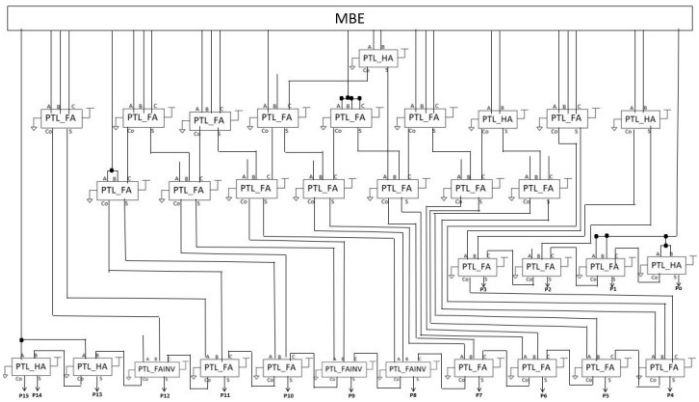

Fig. 8. Proposed Multiplier

Above, the proposed multiplier utilizes Pass Transistor Logic (PTL) Full Adders (FA) and Half Adders (HA) at appropriate positions in the Synthesized Multiplier, with the aim of achieving a low-power and area-efficient design.

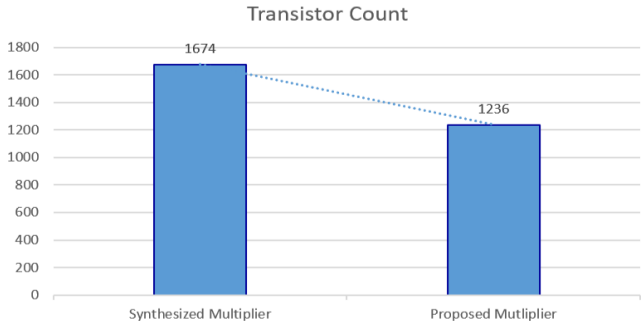

Fig. 9. Comparison of Total Transistor Count

Although including extra PTL_FA can significantly reduce energy consumption, it may also result in an increase in crucial path time. Therefore, achieving an optimal balance between power and speed is essential. In an attempt to bridge this trade-off, we design an optimized multiplier structure as shown in Figure. 8. This is done by introducing four PTL-based Half

Adders (HAs) in the adder tree. This adds power efficiency with minimal performance loss. Moreover, careful placement of PTL-based arithmetic components helps reduce transistor count without compromising accuracy in computation. As illustrated in Figure.9, the proposed a maximum of eight bit signed multiplier consists of 1236 transistors, achieving a 26.16% reduction in transistor count compared to a conventionally synthesized multiplier. These improvements highlight the effectiveness of PTL logic in designing compact, low-power, and high-performance multipliers.

TABLE II
PERFORMANCE ANALYSIS OF DIFFERENT MULTIPLIER ARCHITECTURES

Multiplier	Supply Voltage(V)	Power(µW)	Delay(ps)	Area(µm2)	PDP(fJ)
Synthesized	0.9	144	240.8	144.94	34.67
Proposed	0.9	90.14	160.4	125.44	14.45
[1]	0.9	124	760	749.12	94.24
[9]	0.9	128.89	950.8	1036	121.17

IV. EXPERIMENTAL RESULTS

To compare our design with existing implementations, we design a maximum of eight bit multiplier using Cadence Virtuoso in 45nm, 0.9V standard cell library. We execute the simulations at 27°C with a supply voltage of 0.9V.

Fig.10. (a) Comparison of Power Consumption

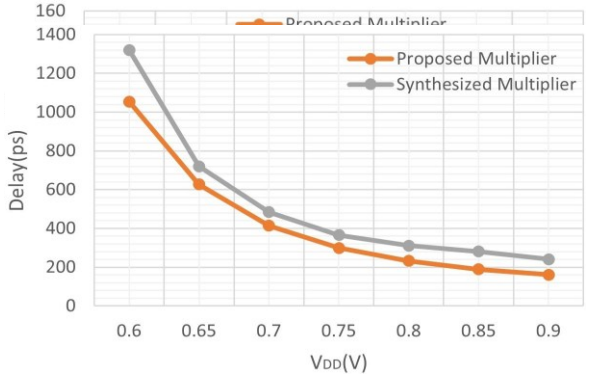

Fig. 10. (b) Comparison of Delay

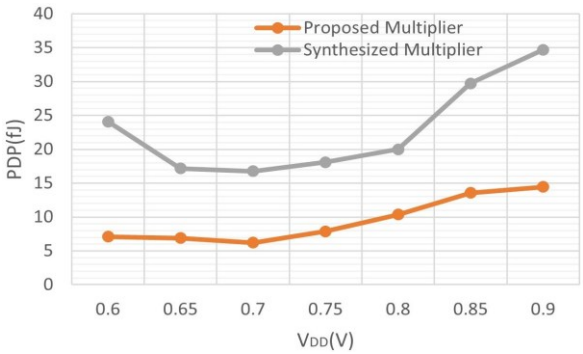

Fig. 10.(c) Comparison of PDP

The power consumption is estimated using 1000 random input patterns at a frequency of 500MHz, and the power-delay product (PDP) is evaluated by multiplying the worst-case delay with the average power consumption of the main circuit. The performance of the multipliers is analyzed over a range of supply voltages (0.5V to 0.9V) at 500MHz. We compare the performance of the proposed multiplier with previously published works [1], [9], summarized in Table II. The stated metrics include delay, area, power usage, and Power Delay Product. The designs in [9] and [1] were initially built on the 65nm technology, and to be fair, they were reduced to 32nm following the technique from [14]. Subsequently, the power-delay data was updated accordingly. As can be seen from Table III, the designed multiplier results in significant improvements compared to the best counterpart, such as 9.72% delay reduction, 13.45% area reduction, 15.19% power reduction, and 23.44% PDP improvement. As shown in Figure. 10(a)–(c), the proposed multiplier performs better than the synthesized one for all supply voltages (0.5V–0.9V) in terms of speed, energy, and PDP. Simulation results in Figure. 10(a) verify that the proposed multiplier works down to 0.5V, and Figure. 10(c) demonstrates that the optimal PDP is obtained at 0.8V.

V. CONCLUSION

In this short, we demonstrate a maximum of eight-bit multiplier utilizing the PTL method. Our experimental results for simulation show the multiplier achieves the PDP values down to an amazing 23.44% as compared with the best among all counterparts. Additionally, across supply voltages, from 0.5V to 0.9 V, proposed multipliers prove faster and of greater energy efficiency while outscoring other designs of multipliers when it comes to power/delay trade-off.

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