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# THE IMPACT OF DIGITAL DELAY LINES' SPATIAL ALLOCATION ON THE DPS SYNCHRONIZATION QUALITY

**Robert Frankowski[1)], Maciej Gurski[1)], Ryszard Szplet[2)]**

*1) Institute of Engineering and Technology, Faculty of Physics, Astronomy and Informatics, Nicolaus Copernicus University in Toruń, ul. Grudziądzka 5, 87-100 Toruń, Poland* (✉ *robef@umk.pl*)
*2) Institute of Communication Systems, Faculty of Electronics, Military University of Technology, ul. gen. Sylwestra Kaliskiego 2, 00-908 Warsaw, Poland*

**Abstract**

The paper concerns the optimization methodology of design of a high-resolution digital phase synchronizer (DPS) module cooperating with a multi-channel coincidence counter. The main function of the DPS module was to ensure high synchronization between the measurement system and trigger pulses (with various repetition rates) from the photo detector. With this approach, it became possible to adapt the measurement system to work with a wide spectrum of excitation sources while maintaining the required metrological parameters. The DPS resolution is determined by the architecture of coding tapped delay lines (TDLs) utilized, whereas the degree of synchronization is determined by the differences in their integral nonlinearity errors ($\Delta R_{\mathrm{INL}}$). In traditional DPS designs, the basis for synchronization were single TDLs built on arithmetic carry chain paths, which are usually characterized by high nonlinearity. The approach presented in this paper assumes the use of complex tapped delay lines (CTDLs) and an appropriate selection of spatial TDLs allocations within a programmable logic structure. The proposed solution enables an effective minimization (from 62.6 ps to 26.2 ps) of the synchronization error between the measurement system and the investigated process.

Keywords: Programmable logic structures, Delay lines, Phase synchronizer, Time interval measurement.

## 1. Introduction

*Field programmable gate array* (FPGA) structures, alongside *application-specific integrated circuits* (ASICs), remain a popular choice for *time to digital converters* (TDCs) implementations [1–9]. The main factors that decide about this are the shorter development time and lower costs than in ASICs, as well as the possibility of reprogramming. An undesirable feature of FPGA-based prototyping is the variation in the time bin sizes of the *tapped delay lines* (TDLs), which leads to nonuniformity and degradation of TDC time resolution. To improve nonlinearity and reduce the size of the bins, the method of comparing time bins of multiple TDLs is usually used [10–14]. Unfortunately, the *complex tapped delay line* (CTDL) architecture needs greater resource requirements and can be difficult to implement in small FPGA structures. The


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recommended solution in this situation may be to increase the time standard frequency and to apply a line selection algorithm [15]. The resolution of the *digital phase synchronizer* (DPS) is determined by the architecture of TDLs, but the quality of the degree of synchronization, by $\Delta R_{\mathrm{INL}}$ errors. In traditional DPS designs [16], the principle of synchronization was implemented based on single TDLs, which were characterized by relatively high nonlinearities. The use of multiple delay lines and an appropriate selection of TDLs spatial allocations [17, 18] within FPGA devices allows for improving the quality of DPS synchronization. This article provides crucial information on the multi-segment digital TDL allocation process used to create CTDLs, preferred to obtain greater time resolution and linearity of the DPS module. The obtained results confirm the validity of the adopted assumptions and the effectiveness of optimizing the DPS implementation process, specifically in terms of increasing its resolution, without the need to change the applied technology.

This article is organized as follows. In Section 2, a simplified block diagram and main information on DPS functionality are presented. The AMD FPGAs series SLICE architecture and global clock network are described in Section 3. This chapter also provides information on the design of multiple delay lines and potential places of their allocation in the FPGA structure. At the end, the TDL segment sorting methods used for bubble error minimization are explained. In the next section, we include the results of experimental tests obtained for four most favourable implementation groups. In each group, a delay line selection algorithm was applied to obtain the optimal implementation of CTDL. In this chapter, the test results, compared to the plain allocation and tuned TDLs implementations, are also described in detail. Finally, we present the segment mapping procedure preferred for the highest quality of DPS synchronization. Finding the optimal CTDL implementation is the main goal of this work.

## 2. DPS architecture

The simplified block diagram of the DPS module is presented in Fig. 1. The basic functional elements of the DPS module are high-resolution TDLs. Such TDLs are the main components for the development of two important DPS sub-modules, namely: the *phase detection module* (PDM) and the *delay selection module* (DSM). The DPS architecture presented in [16] involves the use of two TDLs, one in each of the DPS sub-modules. The approach proposed in this article is based on the CTDL architecture and assumes selecting four TDLs in PDM and two TDLs in DSM modules. The PDM and DSM modules are responsible for precise phase detection of the reference clock signal and ensuring effective synchronization among synchronized signals.

Information about the time relation between the main clock and the trigger pulse is represented at the PDM outputs in a pseudo-thermometric code. Based on this code, the correct mapping procedure in the DSM module is executed using a switching matrix. The required number of TDL segments in both modules is determined by the period of the clock signal, which is the time base of the measurement system. In the case under consideration, the DPS module was clocked with a reference clock signal of 350 MHz obtained from the process of digital frequency synthesis. As regards, the built-in FPGA structure *Digital Clock Manager* (DCM) blocks were used for this purpose. The TDLs resolutions for two flip-flop architecture (placed in SLICE) were approximately 22.5 ps. This implied the use of a TDL line consisting of at least 127 delay segments, respectively. The implementation of CTDL lines increases the number of active delay segments used to build PDM and DSM. The required logical resources typically grow proportionally to the number of TDLs used for CTDL creation.

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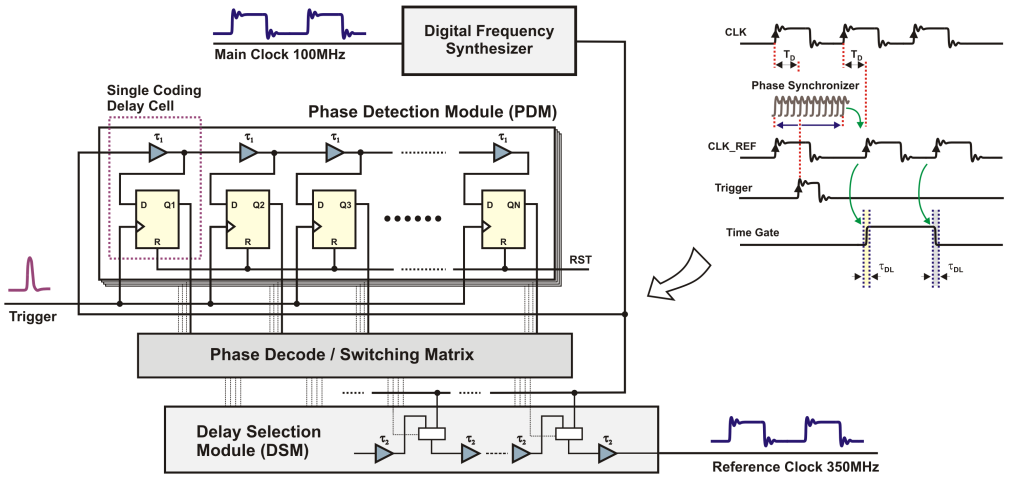


Fig. 1. Simplified block diagram of the DPS module.

## 3. Multiple TDL implementations

*Configurable logic blocks* (CLBs) are basic logic resources intended to implement sequential and combinational circuits in FPGAs. Each CLB block contains four SLICE cells, grouped in two pairs and built-in separate columns of the FPGA (Fig. 2). SLICEs are routed individually by independent carry chain paths dedicated to implement arithmetic functions. The chip columns (marked by the manufacturer with X symbols) are grouped by eight with respect to the areas reserved for the implementation of memory and multiplication blocks.

The global clock lines designed to support high frequency signals spread from the central part of the chip. To achieve uniform even signal distribution and ensure comparable timing parameters across the chip, a mechanism of dividing the structure into clock regions was used. The signal distribution delays obtained within a single clock region and between clock regions (for the GR1-GR4 groups) are shown in Fig. 2a–c. The signals' skew inside the clock regions are comparable and do not exceed more than 25 ps, while between neighbouring segments it is only 5 ps. A completely different situation occurs at the border of clock regions. In this case, the signal skew increases dramatically, reaching 32 ps.

The proposed FPGA architecture allows for the implementation of 32 independent TDLs with 256 taps placed inside the 32 CLBs. Each TDL was built from carry chain components, such as MUXCY and XORCY, used for forming fast arithmetic transfers. The non-standard use of these components, the technological spread of the used resources and also the differences in signal propagation times have a significant impact on the high non-linearity of the transfer characteristics of TDLs, which can lead to bubble errors [19] at the processing stage (Fig. 3b).

Bubble errors may be responsible for the malfunction of the phase decoder, which may return incorrect values during the conversion process [20, 21]. The use of proper TDL segment sorting methods (Fig. 3b) minimizes bubble errors and ensures the correct operation of the DPS module. The procedure for creating CTDL lines (Fig. 3a) requires the determination of the transfer characteristics of the TDLs and the relative shifts $\Delta t_{di}$ between the lines. This procedure is described in detail in [10].

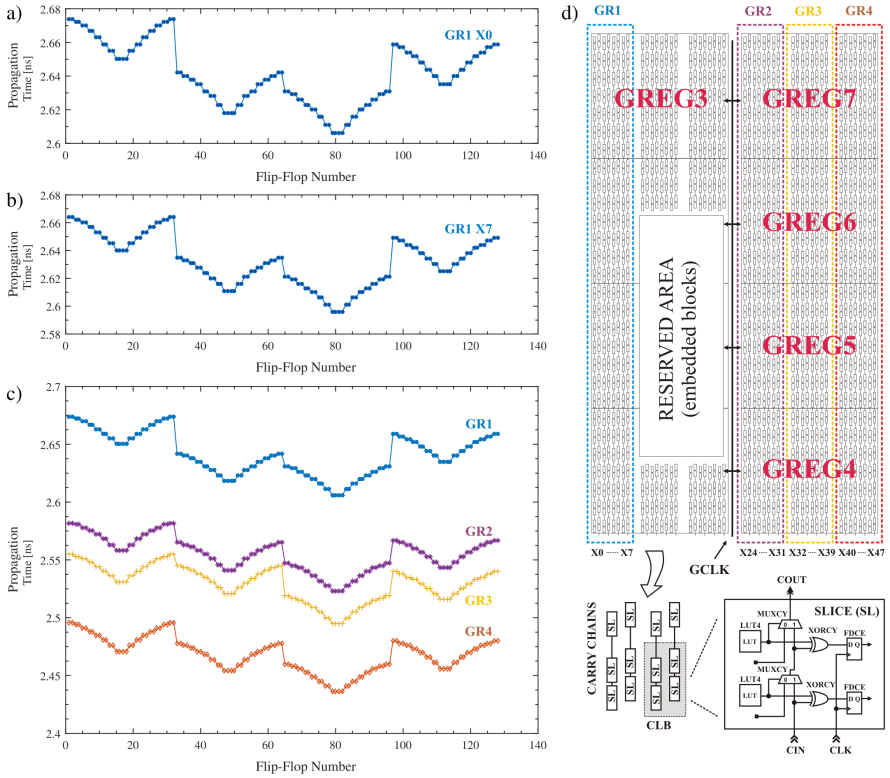


Fig. 2. FPGA device architecture: the skew diagram of clock signal distribution in the GR1 allocation area for selected columns X0 (a) and X7 (b), and then within the GR2, GR3, and GR4 allocation areas (c); device topology, potential TDL allocation groups, and logic resources construction (d).

## 4. Experimental results

Experimental tests, performed to identify the timing parameters of the implemented lines, were carried out using an ML403 hardware platform. In the area of all possible DPS allocations, four most favourable implementation groups (GR1-GR4) were identified. Within each group, eight TDL lines were implemented in the appropriate columns of the FPGA device. The architecture of the XC4VFX12 FPGA device allows the implementation of TDLs with $q_{\mathrm{eqv}}$ resolutions [10] ranging from 26.76 ps to 30.87 ps. The transfer characteristics for three randomly selected TDLs are shown in Fig. 4.

As illustrated in Fig. 4, the TDLs implemented in groups GR1 and GR2 show worse timing parameters (less uniformity of bin widths) than those in GR4. This comes from the fact that the GREG1-GREG2, GREG2-GREG3 and GREG5-GREG6 nonuniformities between clock regions (Fig. 2a–c) do not expand across the GR4 group. Due to the above feature, typical for FPGA technology, it was necessary to identify the correctness of the TDL processing. For this purpose, using the code density test method [22], a series of experimental tests of TDLs were performed. Each time, the states of the FDCE outputs (flip-flops in SLICEs) were recorded directly, bypassing the code converters. Unfortunately, when analysing the test results, bubble errors were detected during

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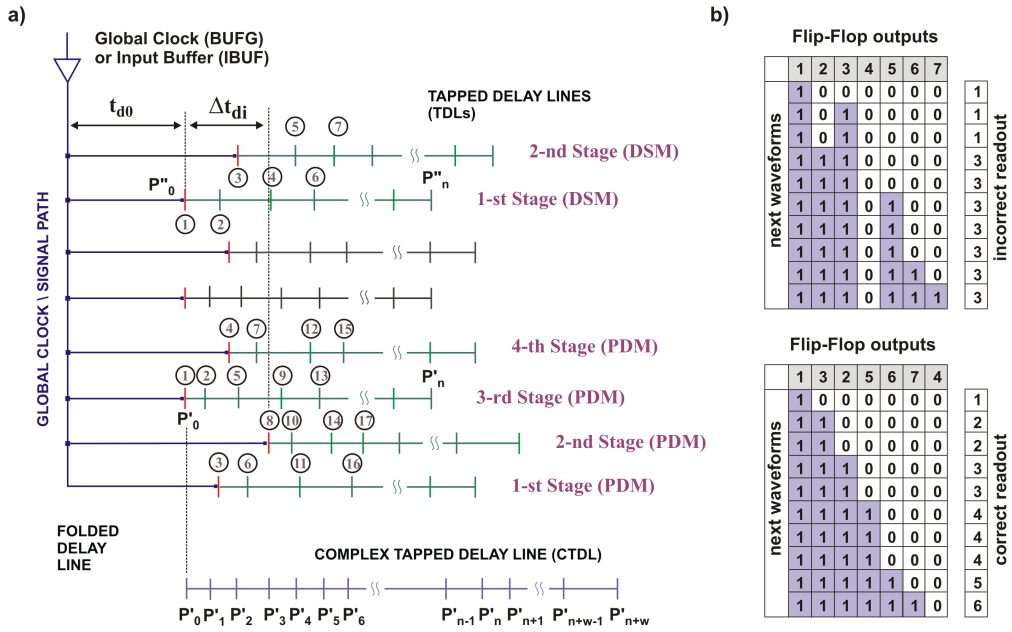


Fig. 3. Multiple delay line creation (a) [10] and the segment sorting procedure (b) [15] used for minimization of bubble errors.

the conversion process. For this reason, an appropriate sorting procedure was carried out according to the scheme shown in Fig. 3b. Finally, the correct orders of the delay segments were established. The values of $q_{\mathrm{eqv}}$ resolution for individual TDL allocation areas are summarised in Table 1.

Table 1. Resolutions $q_{\mathrm{eqv}}$ of the TDLs implemented in eight possible locations.

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **GR 1** | **X0** | **X1** | **X2** | **X3** | **X4** | **X5** | **X6** | **X7** |
| | 29.75 ps | 28.27 ps | 28.71 ps | 28.27 ps | 28.92 ps | 27.88 ps | 27.99 ps | 27.74 ps |
| **GR 2** | **X24** | **X25** | **X26** | **X27** | **X28** | **X29** | **X30** | **X31** |
| | 30.04 ps | 28.84 ps | 28.77 ps | 28.14 ps | 28.79 ps | 29.76 ps | 28.73 ps | 28.45 ps |
| **GR 3** | **X32** | **X33** | **X34** | **X35** | **X36** | **X37** | **X38** | **X39** |
| | 30.87 ps | 28.52 ps | 28.57 ps | 28.95 ps | 28.13 ps | 28.06 ps | 27.45 ps | 29.36 ps |
| **GR 4** | **X40** | **X41** | **X42** | **X43** | **X44** | **X45** | **X46** | **X47** |
| | 26.76 ps | 28.01 ps | 29.30 ps | 28.06 ps | 28.14 ps | 27.37 ps | 27.03 ps | 27.18 ps |

The best performance of TDL allocations was obtained for the GR4 area. For this allocation, no significant deviations in the global clock distribution network delays at the clock domain boundaries are observed. The evaluated average $q_{\mathrm{eqv}}$ resolution value of the TDLs was 27.73 ps, while the averaged maximum of *integral nonlinearity error* (INL) equals 1.7 ps. The TDLs in the GR1, GR2 and GR3 areas were characterized by worse results. Their average $q_{\mathrm{eqv}}$ resolutions were 28.44 ps, 28.94 ps and 28.74 ps.

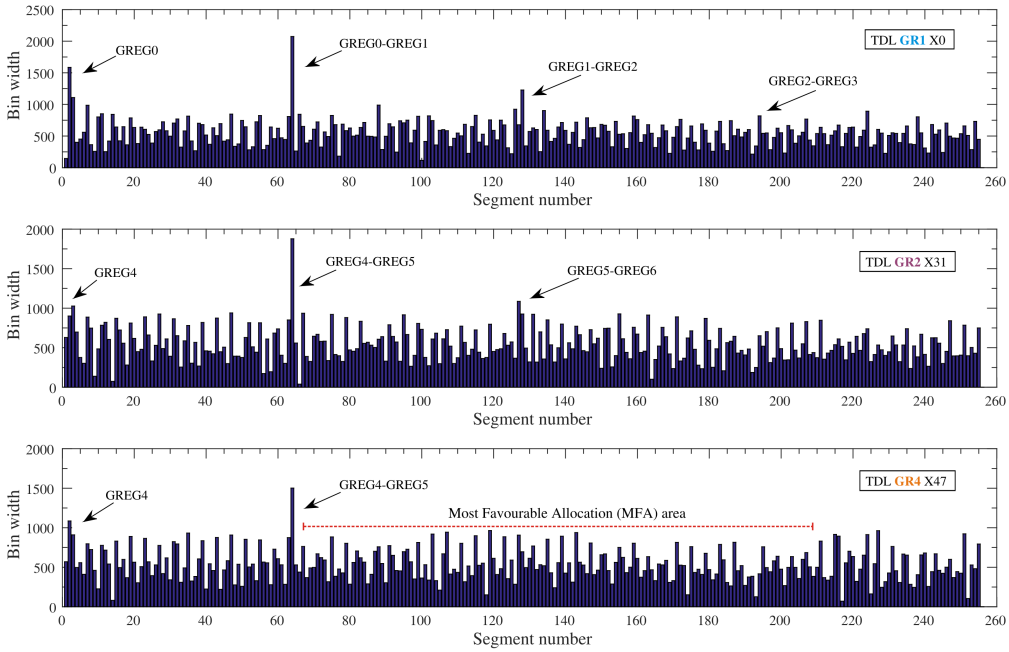


Fig. 4. TDL characteristics for GR1, GR2, and GR4 allocation areas.

The final step in the CTDL formation procedure was to determine the propagation times of the routing signals entering the TDLs. The measurement was carried out for each of the four allocation areas. The results for the selected GR3 and GR4 groups are shown in Table 2.

Table 2. Propagation times $\Delta t_{\mathrm{d}i}$ of paths for two randomly selected groups.

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **GR 3** | **X32** | **X33** | **X34** | **X35** | **X36** | **X37** | **X38** | **X39** |
| | 24.28 ps | 20.11 ps | 5.49 ps | 20.93 ps | 7.60 ps | 0 ps | 32.39 ps | 35.03 ps |
| **GR 4** | **X40** | **X41** | **X42** | **X43** | **X44** | **X45** | **X46** | **X47** |
| | 11.01 ps | 1.56 ps | 13.42 ps | 3.09 ps | 0 ps | 15.72 ps | 21.75 ps | 22.78 ps |

The maximum spreads of propagation times $\Delta t_{\mathrm{d}i}$ obtained for individual groups from GR1 to GR4 were 28.11 ps, 32.26 ps, 35.03 ps and 22.78 ps, respectively. The above scatters have a significant impact on the process of assembling the CTDL lines. As a result of the assembly of TDLs with similar characteristics, *e.g.* with dominant wide bins at the region boundaries, further accumulation of bins with larger widths is observed (Fig. 5).

Of course, the above situation is not always guaranteed. The bin widths, in the best-case scenario, may be divided, while in the worst case, they may accumulate. The first situation may occur when multiple narrow bins from one TDL line are assigned to a wide bin in another line. As a result, such a bin ceases to be dominant in the CTDL characteristics. However, partial coverage of dominant bins increases the probability of accumulation of areas with dominant bin widths. For this reason, it is crucial to select appropriate TDLs by examining all possible configurations.

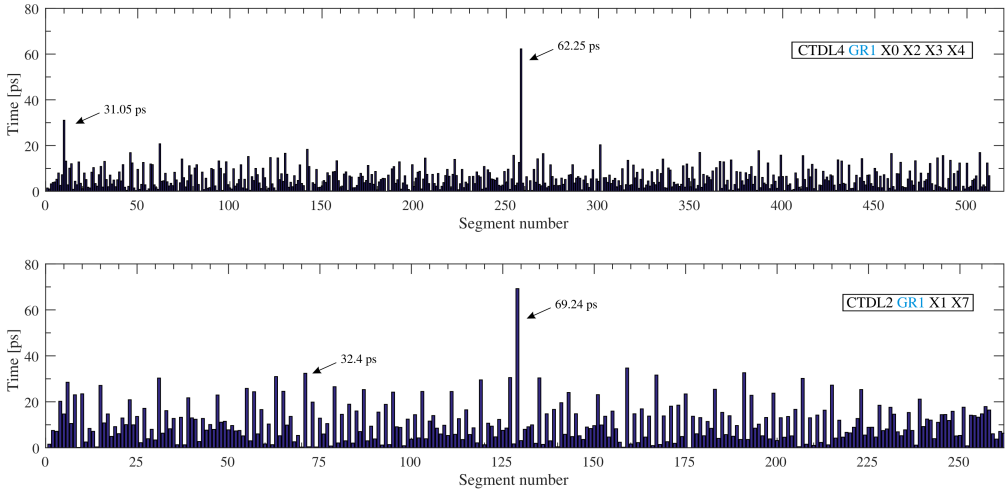


Fig. 5. Bin widths of CTDL4 and CTDL2 placed in the GR1 allocation area.

Achieving a higher resolution of a CTDL requires combining more TDLs. This would be easiest to obtain for eight TDLs in a group due to the single folding of all TDLs (Fig. 6).

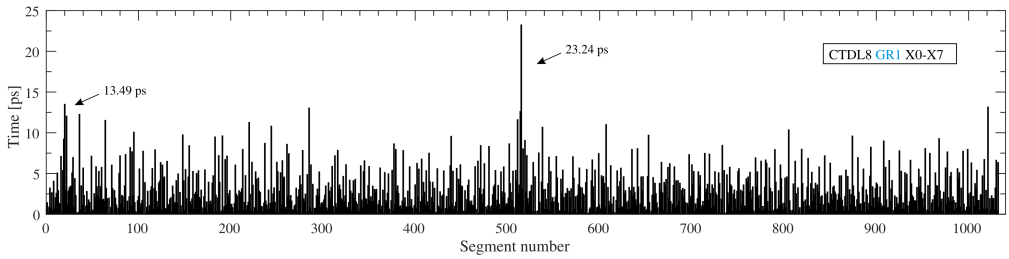


Fig. 6. CTDL8 bin widths placed in the GR1 allocation area.

The situation is more complicated for a smaller number of TDLs (from the set of eight TDLs), where the number of possible line combinations increases. The number of different combinations of four TDLs from an eight-element set is 70, whereas for two TDLs from four possible areas it is smaller and amounts only 6. For this reason, 76 combinations of TDL compositions were analysed for each of the four allocation areas (GR1-GR4).

The conducted research allowed the identification of relationships describing the impact of selecting a specific spatial configuration of TDLs on the parameters of newly created CTDLs. The line selection algorithm applied for this purpose directly checked all possible combinations of TDLs [15]. Based on this, the equivalent resolution limits of the CTDLs used in the implementation of the DPS module were determined. The results are shown in Fig. 7a.

In the graph, the $q_{\mathrm{eqv}}$ resolution results of the CTDL lines (obtained for the GR4 group) are indicated in black. Moreover, the comparative result of implementing a single TDL with $q_{\mathrm{eqv}}$ of 13.26 ps in the Kintex UltraScale XCKU040 device is also plotted there (dashed line). To obtain consistent results, the selection of four TDLs in group GR4 is sufficient, but the use of three TDLs may not be guaranteed (Fig. 7a).

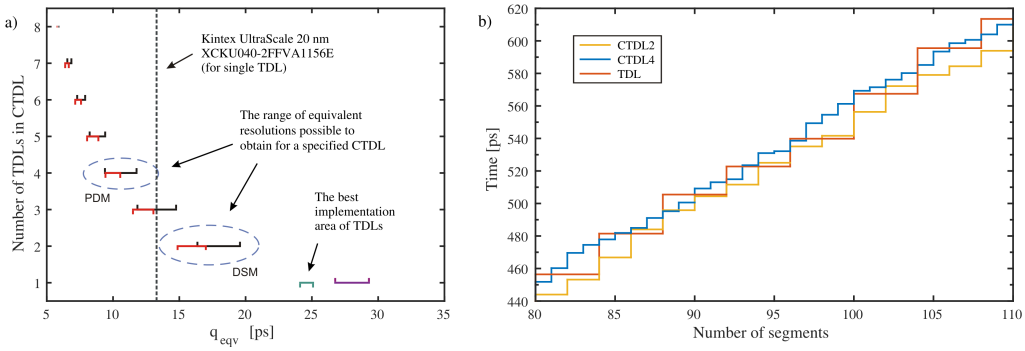


Fig. 7. CTDL equivalent resolution $q_{\mathrm{eqv}}$ vs the number of TDLs involved (a) and the results of segment mapping in the PDM and DSM sub-modules (b).

The best TDL configurations and the parameters of the newly created CTDLs for the specified allocation areas are summarised in Table 3.

Table 3. Best TDL configurations and CTDL timing parameters.

| Allocation area | The best configuration in the PDM module | The best configuration in the DSM module | Equivalent resolution for CTDL in PDM | Equivalent resolution for CTDL in DSM |
|---|---|---|---|---|
| Group 1 | [X3, X4, X6, X7] | [X1, X2] | 9.75 ps | 16.78 ps |
| Group 2 | [X25, X27, X29, X30] | [X24, X31] | 9.97 ps | 17.69 ps |
| Group 3 | [X32, X35, X36, X37] | [X34, X39] | 9.42 ps | 16.66 ps |
| Group 4 | [X40, X41, X46, X47] | [X43, X45] | 9.45 ps | 15.65 ps |

Example characteristics of CTDL4 and CTDL2 obtained for the most favourable TDLs implemented in the GR2 allocation area are shown in Fig. 8.

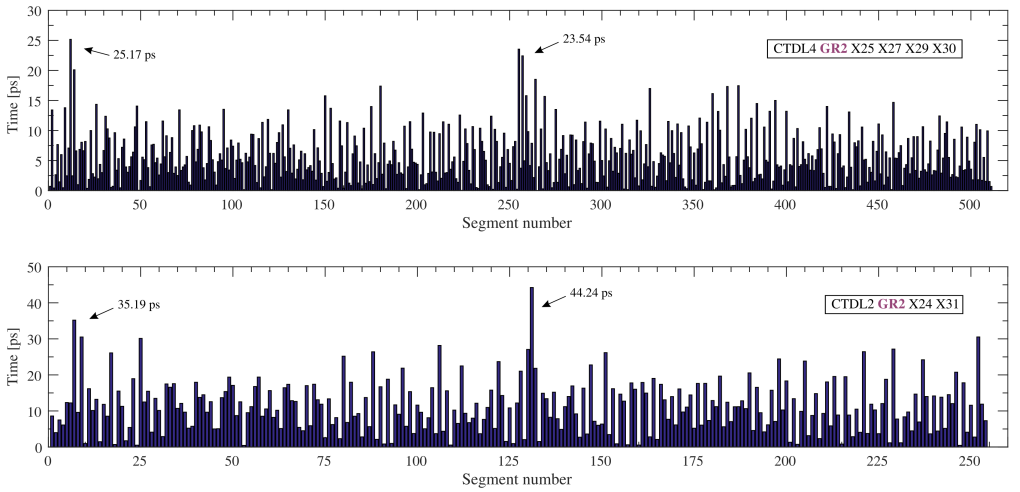


Fig. 8. Bin widths of CTDL4 and CTDL2 placed in the GR2 allocation area.

The probability of accumulation of areas with dominant bin widths observed in Fig. 8 remains still noticeable, but not as significant as in Fig. 5. The implementation of four and two TDLs in the PDM and DSM modules allowed achieving resolutions of 9.97 ps and 17.69 ps, respectively. The best composition of four TDLs (CTDL4) yields 511 delay segments, but a composition of two TDLs (CTDL2) yields only 254. This situation is consistent with the fact that, for CTDL transfer characteristics with predominantly larger bin widths, a smaller number of delay segments is required to cover the same range. This is particularly evident when the transfer characteristics are highly non-linear.

The subsequent optimisation process concerned the selection of allocation within the GR4 group with the most favourable timing parameters. By implementing the TDLs within the area indicated in Fig. 4 (red dashed line), the average $q_{\mathrm{eqv}}$ resolution value of 24.58 ps was obtained. The CTDL4 line built at this location had approximately 543 delay segments. The difference in the number of required segments was mainly caused by the additional wide bins in the initial line segments (GREG4) which had to be split into more segments with shorter times in the target allocation. Example characteristics of CTDL4 and CTDL2 obtained for TDLs implemented in the GR4 MFA allocation area are shown in Fig. 9.

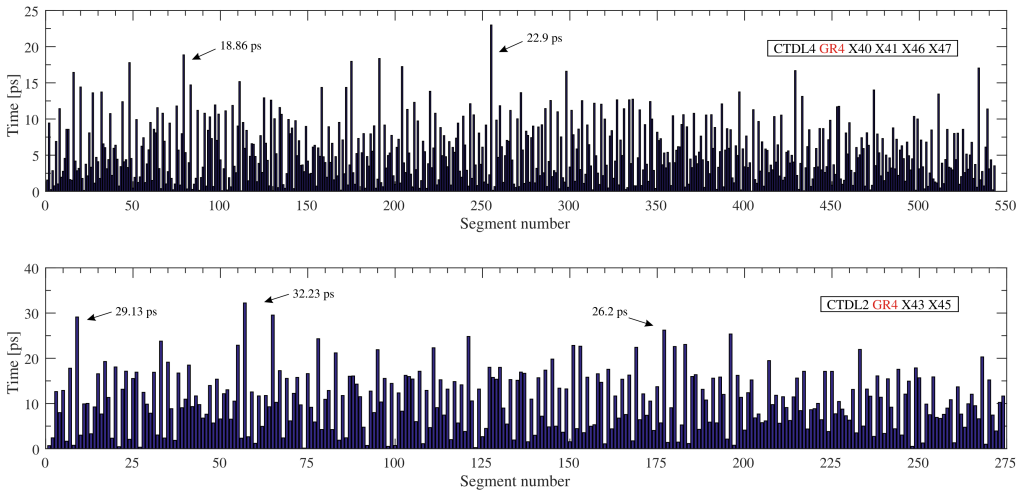


Fig. 9. Bin widths of CTDL4 and CTDL2 placed in the GR4 MFA allocation area.

The best $q_{\mathrm{eqv}}$ resolution results of the CTDL lines obtained for the GR4 MFA group after omitting the first 64-line segments are also indicated in Fig. 7a (red line). To obtain results consistent with the Kintex UltraScale structure, the use of three TDLs would be required, while the selection of four TDLs makes it possible to achieve resolutions of 9.4 ps.

The cross-mapping of CTDL line segments in the PDM and DSM is the basis for synchronisation of the DPS module (Fig. 7b). This procedure involves assigning PDM to those DSM segments for which the delay mismatch errors will be the smallest. The highest degree of synchronisation is achievable for ideal TDLs with the same resolution. For real TDLs, it is necessary to identify the INL errors of both modules. The differences in INL errors are responsible for the precision of the time interval mapping by the DSM module. For experimental purposes, in the first approach, measurements were performed for single TDL lines. The differences determined for integral nonlinearity errors $\Delta R_{\mathrm{INL}}$ (for two flip-flop architecture) did not exceed 23.1 ps. The associated maximum range of all non-linearity values reached about 36.5 ps in this case.

The test results for the best CTDL configuration are shown in Fig. 10a. The maximum value of the differences between the nonlinearity errors of CTDLs was in this case 8.6 ps. The obtained maximum range of the determined $\Delta R_{\mathrm{INL}}$ differences was 16.7 ps, whereas its average value was equal to 2.85 ps.

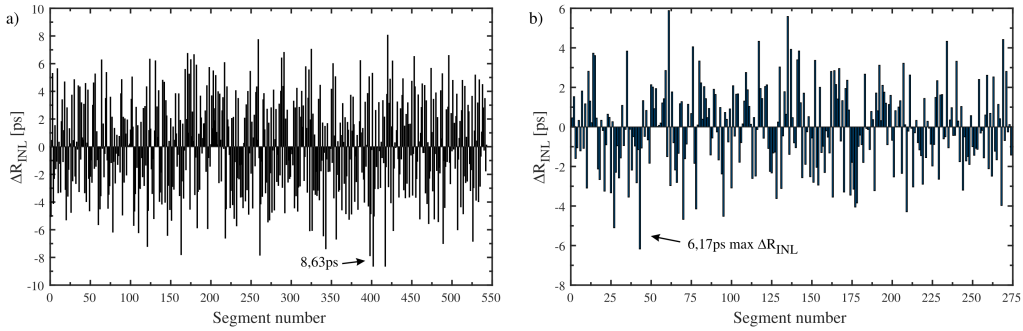


Fig. 10. Synchronization results for all (a) and the most favourable (b) routings.

By limiting the mapping to the most favourable routes only, the above $\Delta R_{\mathrm{INL}}$ values were compensated to approximately 6.2 ps. The maximum range of all non-linearity values and mean values were 12.1 ps and 1.65 ps, respectively. The result of the final compensation is shown in Fig. 10b.

## 5. Conclusions

As shown in this paper, the use of the TDL selection algorithm allows us to obtain better $q_{\mathrm{eqv}}$ resolution without incrementing the required hardware resources. Determined relations between the $q_{\mathrm{eqv}}$ and the number of TDLs allow us to estimate the upper limit of resolution that can be achieved for a given FPGA chip. The implementation of eight TDLs allows us to achieve a resolution of 5.74 ps, which is an improvement of 7.56 ps compared to the implementation of a single TDL in the Kintex UltraScale device. This research provides an opportunity to restore the oldest solutions to parameters comparable to implementations in newer FPGA structures. In this way, the DPS module optimization process allowed for improvement of synchronization which is almost seven times better compared to ordinary implementations. This was done at the cost of additional logical resources necessary to build the CTDL line. Importantly, randomly combined TDLs only sporadically improve the CTDL performance. Therefore, the random TDLs configuration providing parameters similar to those of Kintex UltraScale TDL required the use of three TDLs implemented in the MFA area (Fig. 7a). Implementation outside this area requires the use of four TDLs configured randomly. Using the best TDL configurations (chosen according to the line selection algorithm) allows us to reduce the required number of TDLs to three, regardless of whether they are implemented in the MFA area. The above number of TDLs is acceptable for implementations in small FPGA structures.

The ranges of $q_{\mathrm{eqv}}$ achievable with a fixed number of TDLs are particularly important from the perspective of developing the DPS module. The TDL selection method used in this paper identified the potentially best allocation for placing a DPS module in the programmable structure. The tests were performed for the XC4VFX12 device. Four areas of possible DPS module allocations were investigated. Choosing the right spatial allocation and the use of multiple lines in the selected region

allowed for at least a 70% improvement of $q_{\mathrm{eqv}}$ resolution and ensured effective minimization of $\Delta R_{\mathrm{INL}}$ differences from 23.1 ps to 6.2 ps. This reduced the synchronization error of the DPS module from 62.6 ps up to 26.2 ps.

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**Robert Frankowski** received the M.Sc. degree in physics (specialty: physical basics of microelectronics) from the Nicolaus Copernicus University (NCU), Torun, Poland, in 2001. In 2011, he received the Ph.D. degree in Technical Sciences from the Warsaw University of Technology. From 2006 to 2008, he participated in experiments conducted at the National Laboratory for Atomic, Molecular, and Optical Physics. In 2009 he received the team Award of the Rector of the NCU for Scientific and Research Activities for developing the methodology for the design and verification of accurate time interval measurement systems. He is currently an Assistant Professor at the Institute of Engineering and Technology, NCU, Torun, where he leads the Metrology and Measurement Systems research group. He has authored and co-authored more than 20 papers in the field of precise time interval metrology, primarily involving FPGA-based solutions. His main research interest is designing precision measuring and control systems integrated in FPGA and MPSoC technology used for specific applications in many branches of science.

**Ryszard Szplet** received the M.Sc. degree in electronic engineering and the Ph.D. and habilitation degrees in applied sciences from the Military University of Technology (MUT), Warsaw, Poland, in 1989, 1997, and 2013, respectively. From 2000 to 2001, he spent one year as a researcher with the University of Oulu, Oulu, Finland. He is currently Full Professor with the MUT (title obtained in 2019), where he also heads the research team of precise time metrology. In the years 2020-2024 he held the position of Dean of the Faculty of Electronics at the MUT. He is a member of the Committee on Metrology and Scientific Instrumentation of the Polish Academy of Sciences (PAS). He also serves as editor-in-chief of the international journal Metrology and Measurement Systems. He has been involved in various research projects, sponsored by both public and private funds. He has authored or coauthored more than 150 papers appearing in international journals and conference proceedings. His current research interests include fast digital electronics and methods and techniques for precise time metrology, especially instrumentation for advanced time interval and frequency measurements.

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**Maciej Gurski** was born in Toruń, Poland in 1977. He received his M.Sc. degree in 2002 from Nicolaus Copernicus University in Toruń and his Ph.D. degree from the Military University of Technology (MUT), Warsaw, Poland, in 2024. His main research interest is developing precise methods and instruments for time metrology and control systems in FPGA technology.