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# HIGH-PRECISION 3-CHANNEL TIME INTERVAL COUNTER IN A LOW-COST AMD SPARTAN-7 FPGA

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**Abstract**

This paper presents the design, implementation, and performance evaluation of a 3-channel integrated time interval counter implemented in a low-cost Spartan-7 (AMD/Xilinx) FPGA device. Based on a hybrid measurement approach that combines timestamping and two-stage interpolation, the proposed solution provides high metrological parameters, such as: time resolution (2 ps), measurement precision (better than 8 ps) and range (up to 1 h). To achieve high resolution and reduce nonlinearity of the time-to-digital converters (TDCs) involved, the multi-edge coding in four independent tapped delay lines (TDL) was applied. An improved encoder eliminates bubble errors and compresses raw TDL data with limited logic overhead. The integrated code processor performs real-time calibration based on the statistical code density test (SCDT). Implemented within a low-end FPGA chip, the time counter occupies approximately one-third of available logic resources and consumes around 0.5 W. Experimental evaluation confirms the system's potential for cost-effective, high-performance time interval measurements in portable instrumentation.

Keywords: time interval measurement, time interval counter, time-to-digital converter (TDC), field-programmable gate array (FPGA).

## 1. Introduction

Precise time interval and frequency measurements are important in an expanding range of applications, including the creation and distribution of stable time scales, navigation systems, and high-energy physics experiments [1–3]. The requirements on time counters are also constantly increasing. However, because of these high requirements, the number of high-precision measurement instruments available is very limited. The offer is dominated by large, energy-consuming, and expensive desktop time counters [4–7]. As a supplementary proposal, just a few portable counters appear [8–10]. These counters not only match the former ones in terms of high metrological parameters, but they are also pocket-sized, consume little energy, are easy to use and much cheaper. Consequently, these devices have garnered significant interest and are now widely adopted in professional time and frequency laboratories. Advances in microelectronics further enable the replacement of large stationary counters with smaller, portable alternatives that boast superior parameters.


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The measurement core of many modern time interval counters is based on *field-programmable gate arrays* (FPGAs). These programmable logic devices provide high flexibility, low cost, and rapid deployment while maintaining relatively high performance. To achieve high resolution and precision across a broad measurement range, FPGA-based counters often incorporate the interpolation method with high-resolution time-to-digital converters (TDCs) [2,3]. Among many *time-to-digital conversion* techniques, solutions based on *tapped delay lines* (TDLs) remain prevalent and continue to be adapted for newer FPGA chips [11–13]. Although mainstream FPGAs offer increasingly extensive logic resources, many dedicated functional blocks remain underutilised in time interval measurement systems. Users often pay extra cost for faster chips with surplus logic capacity, which increases power consumption and design complexity. This has driven efforts to maximise the performance of time interval measurement systems implemented in small, low-cost FPGAs [14–17].

In this paper, we propose a 3-channel integrated time interval counter implemented in a compact, low-cost AMD/Xilinx Spartan-7 FPGA device. By leveraging state-of-the-art TDC techniques, we demonstrate that high-performance time-interval measurement systems can be realised in programmable logic devices, enabling their practical deployment in pocket-sized instruments.

## 2. Measurement method

An easy way to measure time intervals is to count the reference clock periods of a known frequency. The higher the frequency, the better the measurement resolution achieved. If the binary counter operates continuously and the occurrence of an event (in the form of an edge of an electrical signal) does not cause it to start or stop, but only to register its current state ($N$), then it is called the timestamping method. In such a solution, the period counter can be shared by multiple channels to form a common, coarse timescale for recording events. This allows us to specify time intervals between any registered timestamps (TS). Although the method provides great flexibility and a wide measurement range, its resolution is limited by the clock signal period ($T_{\mathrm{CLK}}$). In practice, it is limited to nearly 1 ns for the newest FPGAs families. To reduce dynamic power consumption, the clock frequency in the proposed design must be also decreased. TDCs are known to achieve several orders of magnitude better resolution but have a limited measurement range. The advantages of both solutions are combined in the interpolation method [18].

### *2.1. Timestamps and two-stage interpolation*

The operation of a timestamp and two-stage interpolation-based counter is illustrated in Fig. 1. The TDC measures the interval ($T_{\mathrm{TDC}}$) between an input pulse rising edge and the nearest rising edge of the main clock signal. The *first interpolation stage* (FIS) determines whether the event occurred in the first half (0° phase) or second half (180° phase) of the clock period ($T_{\mathrm{FIS}}$). This reduces the operating range of the *second interpolation stage* (SIS) by half. Thus, the SIS can quantize the time interval ($T_{\mathrm{SIS}}$) within half the clock period with picosecond-level precision and reduced logic resource usage. The final TS value is calculated as follows:

$$\mathrm{TS} = N \times T_{\mathrm{CLK}} - T_{\mathrm{FIS}} - T_{\mathrm{SIS}}. \tag{1}$$

While multi-stage in-period interpolation (*e.g.*, two-stage) complicates the counter design [19], it can reduce logic resource consumption. With multi-stage interpolation also a lower frequency clock can be used. Both aspects result in reduced power consumption, which is essential for pocket-sized devices.

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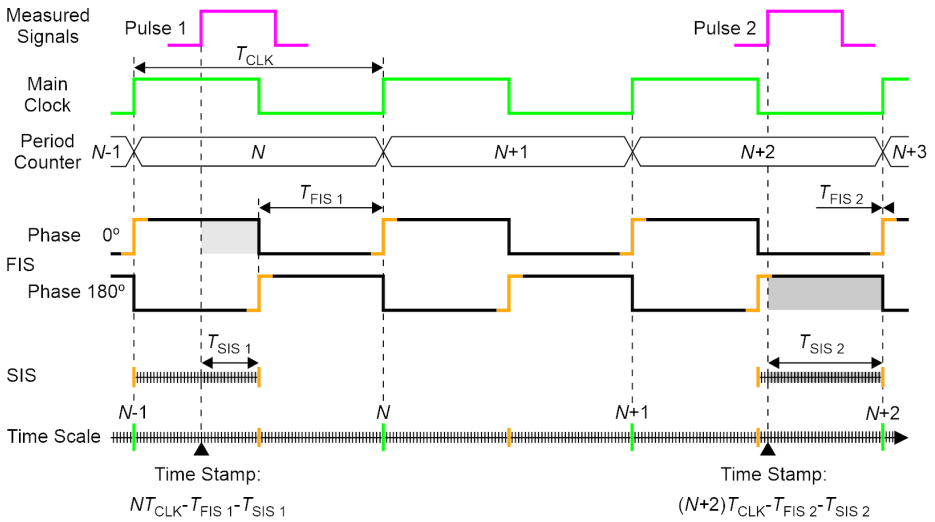



Fig. 1. Measurement method – timestamps with two-stage interpolation.

### *2.2. Multi-edge coding in independent coding lines*

A common TDC architecture employs a *time coding line* (TCL), which combines a TDL with a register (Fig. 2). Here, a single delay buffer connected to a *flip-flop* (FF) is called a delay cell. The start signal propagates through the TDL, reaching successive FF inputs with a delay proportional to the buffer's propagation time ($\tau$), while the stop signal captures the state of the TDL in the register. In FPGAs, such a design is often implemented using carry chains [3], which minimise interconnection delays, but suffer from significant nonlinearity. The delay introduced by a single delay cell (referred to as bin size) can vary from a few to tens of picoseconds due to factors such as technological spread, FPGA granularity, inhomogeneities in the clock signal distribution network, metastability, and *process-voltage-temperature* (PVT) variations.

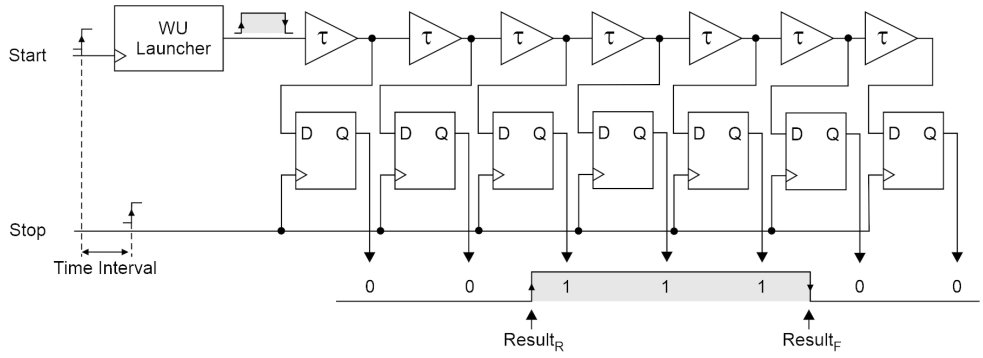



Fig. 2. Wave union (WU) TDC.

To mitigate this nonlinearity and improve resolution beyond the average delay line resolution ($\tau$), two methods are often adopted: the multi-TCL method [20, 21] and the *wave union* (WU) method [22]. Identical TCLs implemented on the same FPGA device exhibit unique transfer

functions due to intrinsic delay variations, enabling them to be treated as independent measurement units. The results of multiple TCLs can be averaged or algorithmically fused (*e.g.*, [23]) to improve resolution. In the WU method, a pulse generator (WU launcher) initiates multiple pulses to propagate along the TDL upon detecting a start signal edge, which is shown in Fig. 2. This creates multiple logic transitions ('0' to '1' and '1' to '0') in the register, allowing multi-edge coding. If one pulse edge encounters a large bin, another edge may intersect a narrower bin, statistically improving resolution and precision.

The multiple TCL method requires considerable logic resources, while the WU method is more difficult to implement and requires a complex encoder to identify transitions. In particular, the more edges are generated by the WU Launcher, the longer the TDL and the more complex the encoder must be. However, these methods can be combined to achieve significant improvements in TDC performance while minimising system complexity, and this is known as multi-edge coding in independent TCLs [24].

## 3. Integrated time interval counter

A block diagram of a single measurement channel of the designed integrated time counter, which combines timestamping and interpolation methods, is shown in Fig. 3. The input circuit consists of a D-type FF that sets a high logic state at the output upon the rising edge of the measurement signal and maintains it until the end of the conversion process. A two-stage TDC measures the time interval within a single main clock period. First, the FIS identifies the main clock signal phase (0° or 180°) and generates a phase-synchronised pulse. Then, the SIS accurately measures the time interval between the edge of the measurement signal and the phase-synchronised edge produced by the FIS. This synchronised pulse is also used to latch the current state of the period counter into a period register. The period counter is implemented as a 40-bit binary counter, driven by a 300 MHz main clock. As a result, it provides a measurement range of up to one hour before overflowing. Raw results from the FIS and SIS are processed in the code processor, which performs the following functions: (1) compresses the obtained results ($T_{\mathrm{FIS}}$, $T_{\mathrm{SIS}}$), (2) executes calibration procedures to identify the TDC transfer function, and (3) calculates values of timestamps based on calibration results. The final results are stored in a *first-in, first-out* (FIFO) memory.

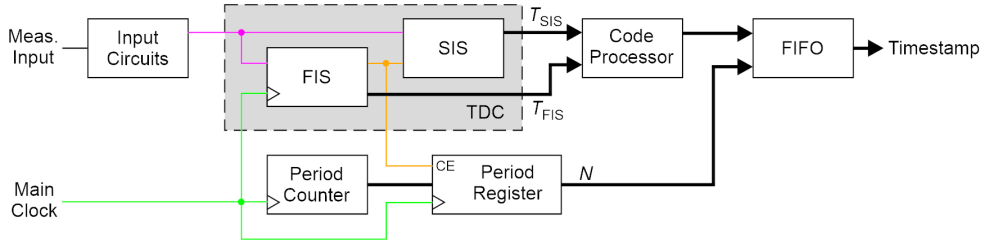



Fig. 3. Single measurement channel of the integrated time interval counter.

### 3.1. Time-to-digital converter design

The design module that largely determines the performance of the integrated time interval counter is the TDC, which design is shown in Fig. 4. The FIS consists of two double-synchronisers clocked at opposite edges of the clock signal. These synchronisers minimise the probability of metastable states and are interconnected via *clock enable* (CE) signals. In the idle state,

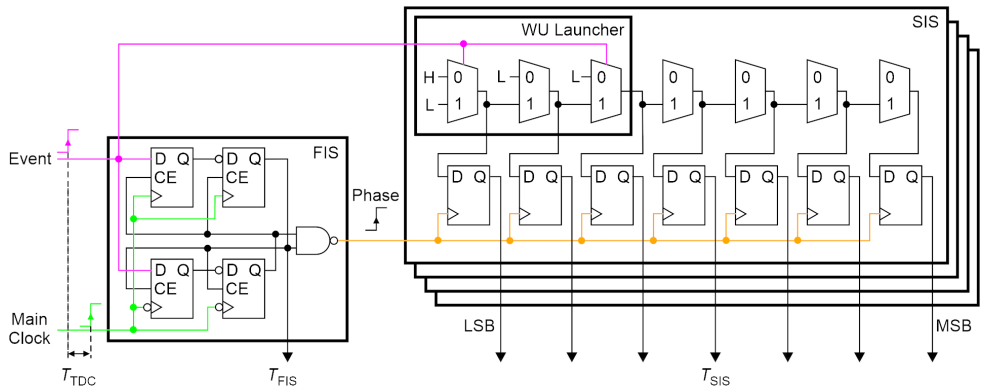



Fig. 4. Two-stage TDC design.

both synchronisers produce a logic '1' at the output, setting the phase signal to '0'. If one of the synchronisers detects a high logic level at its input, it disables the operation of the other and triggers a transition on the phase signal. This edge is subsequently used to latch the current state of the TDL in the SIS.

The TDL is implemented using carry-chain multiplexers, which provide the shortest propagation delay among all FPGA components due to their optimised internal structure and direct routing paths that bypass general-purpose switching matrices. The WU launcher consists of 20 multiplexers, all configured (except the last one) to output a high logic level. A transition on the event signal toggles the first and last multiplexers, generating a single pulse that propagates along the TDL. The pulse width is proportional to the number of multiplexers and their propagation delays. This design enables precise control over the WU pattern while minimising the usage of logic resources when integrating the TDL and launcher.

The complete TDL comprises 148 carry-chain multiplexers. However, due to the presence of the WU launcher, only 128 are used for the first edge. Assuming an average propagation delay ($\tau$) of approximately 16 ps per multiplexer in the Spartan-7 FPGA (speed grade –2), the SIS measurement range is slightly longer than 2 ns (~2.048 ns). Given the main clock frequency of 300 MHz and the use of a two-phase clock in the FIS, this allows coverage of half the clock period (1.66 ns) while leaving a safety margin for clock phase mismatches and PVT variations.

Proper distribution of the clock signal to the FFs is crucial for the correct operation of the converter. In the TDC, two clock signals are used: the main 300 MHz clock (marked green in Fig. 4), which is delivered to the FIS, and a clock signal generated by the FIS (marked orange in Fig. 4), which drives the FFs in the SIS. Both signals are distributed within the FPGA using dedicated clock routing paths, which limits clock skew to tens of picoseconds [25,26]. The selection of the active clock edge takes place directly at the clock input of the FFs.

The discussed WU-based TDL is replicated in the described TDC four times. With two-edge encoding applied across four independent TDLs, the overall measurement resolution improves by a factor of eight compared to a classic TDL (*i.e.*, a single TDL connected to a register). Additionally, the encoding of results is simplified, as discussed in the next subsection. This configuration generates $4 \times 148$ bits of raw data, where the position of eight transitions is critical to determining the time interval ($T_{SIS}$). Consequently, data compression (encoding) is the first processing step followed by conversion of the compressed data into a time value. Both operations are performed by the code processor.

### 3.2. TDC encoding and code processing

The first task of the code processor is data compression, accomplished by an encoder. The encoder identifies the positions in the SIS data where logic state transitions occur and then derives a single compressed value from multiple transitions across multiple lines. The structure and operating principle of the encoder are presented in Fig. 5.

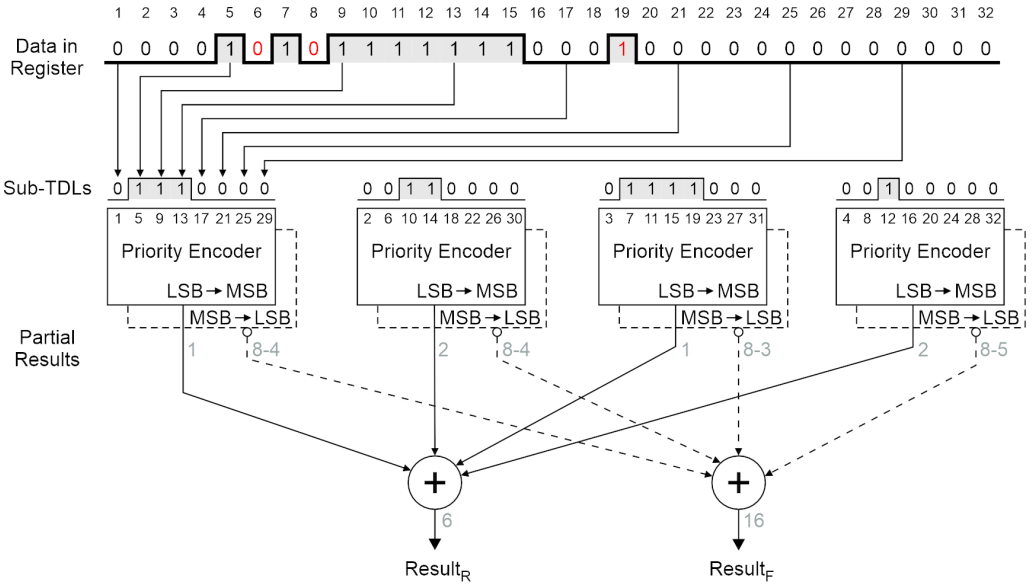



Fig. 5. Block diagram and operation principle of the SIS encoder.

In TDCs employing TDL architectures, a common issue is the occurrence of bubble errors. These errors arise when the measured time interval corresponds to a region in the delay line where the transition between logic states is not a clean single-step boundary. Instead, discontinuities appear in the thermometric code due to timing mismatches, noise, or metastability in the delay elements (in Fig. 5 such errors are marked in red in the data from a single SIS register). A simple and effective solution is to virtually decompose the result into partial results (sub-TDLs) [27, 28]. Each sub-TDL consists of every $k$-th bit from the original TDL result, where the value of $k$ is chosen based on the maximum number of bits over which a bubble error can occur (four in this work). Following this decomposition, each sub-TDL is free of bubble errors. This method is straightforward in its implementation – requiring only the re-routing of certain signals – and highly effective, as it virtually eliminates all bubble errors.

Once the results are free of bubble errors, the encoder searches for the transitions ‘0’–‘1’ and ‘1’–‘0’. Identifying multiple edges can be relatively complex [29, 30]. Therefore, we have limited the process to only two edges per TDL. These edges are identified by two priority encoders operating in opposite directions: one from the *most significant bit* (MSB) to the *least significant bit* (LSB), and the other in reverse order. This approach significantly simplifies the data encoding process. The longer the time interval, the higher the value of the ‘0’–‘1’ transition position and the lower the value of the ‘1’–‘0’ transition position. Consequently, the output of the MSB-to-LSB priority encoder is inverted (converted to the complement code). Finally, the results of both transitions, obtained from all four WU-based TDLs, are summed together.

In the next step, the code processor translates the values obtained from the FIS and SIS into the time values. This translation is performed using the built-in *block random access memory* (BRAM), which stores the transfer characteristics of the interpolators, and results in numerical outputs representing fractions of a clock period with sub-picosecond resolution ($3.33\ \text{ns} / 2^{14} \approx 0.2\ \text{ps}$). In addition, the code processor incorporates algorithms for updating the transfer characteristics during the calibration process, based on the *statistical code density test* (SCDT) [31]. Calibration is initiated automatically at each start-up of the system or manually upon request of the user. This approach enables the device to maintain high measurement precision under varying environmental conditions. The hardware implementation of the calibration algorithms brings several benefits: reduced calibration time, lower data transfer requirements to the host computer, and simplified control software [32].

### *3.3. Integrated time counter implementation*

The integrated time interval counter was implemented in a mid-sized *Spartan-7* (XC7S50) FPGA device from AMD/Xilinx. Spartan-7 chips are among the simplest and smallest in the 7 series, notably lacking gigabit transceivers and a PCI interface. This minimalistic design contributes to their low cost and low power consumption, but they are also a bit slower than other AMD/Xilinx chips such as Artix, Kintex, or Virtex devices. Nevertheless, Spartan-7 FPGAs provide sufficient resources and capabilities to implement high-performance time interval counters.

Each measurement channel was implemented within a single clock region. Special care was taken to precisely locate the FIS within the programmable array – the two synchronisers were positioned close to each other and the routing paths to the NAND gate were manually aligned. This careful placement was essential to ensure that both phases of the clock signal remained equal and that good synchronisation with the SIS was maintained.

Table 1 summarises the utilisation of logic resources of the counter in the Spartan-7 FPGA. In general, the complete design occupies about one-third of the available programmable logic blocks (slices) on the chip. Approximately half of the consumed resources (including slices, *look-up tables* (LUTs), and FFs) are used by the SIS and the encoder (a part of the code processor), which are duplicated across three channels. If only a single-stage interpolation with a TDC based on two-edge coding across four independent lines were used, the TDL length would need to be doubled to cover the main clock period, significantly increasing resource consumption. The BRAM module is used to store the TDC transfer characteristics and implement a FIFO memory, which buffers timestamps before they are sent to the control computer via a USB interface. In addition, the counter integrates several other controllers for the external frequency synthesiser, calibrator, USB interface, and other peripherals. These modules involve additional use of logic resources.

Table 1. Summary of logic resource utilization of the integrated time interval counter.

| | **Slice** | **LUT** | **LUTRAM** | **FF** | **BRAM** |
|---|---|---|---|---|---|
| **Available** | 8150 | 32600 | 9600 | 65200 | 75 |
| **FIS** (×3) | 2 (6) | 3 (9) | 0 | 4 (12) | 0 |
| **SIS** (×3) | 148 (444) | 0 | 0 | 592 (1776) | 0 |
| **Encoder** (×3) | 342 (1026) | 953 (2859) | 0 | 594 (1782) | 0 |
| **Full Design** | 2885 | 6819 | 229 | 7233 | 15.5 |
| **Utilisation** | 35.4% | 20.9% | 2.4% | 11.1% | 20.7% |

Table 2 presents the current consumption of the designed integrated time interval counter, focusing on the FPGA chip only. While the 300 MHz main clock drives the period counter, register, and FIS (in all three channels), the remaining modules operate under a 100 MHz system clock. The complete timestamp processing – from raw data acquisition to the final time value – introduces a dead time of approximately 40 ns per measurement channel, corresponding to a maximum measurement repetition rate of 25 MSa/s per channel. Based on these parameters, power estimates were obtained using the Vivado software tool. The total estimated current consumption was 135 mA, corresponding to a power consumption of approximately 181 mW (assuming a typical core voltage), with a medium confidence level. To verify these values, 25 MHz signals were connected to all three input channels, and current consumption was measured using an FNB58 USB tester from FNIRSI. The actual current consumption was slightly lower, around 113 mA, but since it was drawn from a 5 V USB supply, the measured power consumption amounted to approximately 565 mW.

Table 2. Summary of power consumption of the integrated time interval counter.

| | | **Estimated** | | **Measured** | |
|---|---|---|---|---|---|
| | | Current [mA] | Power [mW] | Current [mA] | Power [mW] |
| **Dynamic** | Clocks | 31 | 31 | 67 | 335 |
| | Signals | 14 | 14 | | |
| | Logic | 12 | 12 | | |
| | BRAM | 22 | 22 | | |
| | I/O | 9 | 25 | | |
| | XADC | 1 | 2 | | |
| | Total | 89 | 106 | | |
| **Static** | | 46 | 75 | 46 | 230 |
| **Total** | | **135** | **181** | **113** | **565** |

The supply voltage, and particularly its noise, has a significant impact on the performance of the integrated time counter. Due to high levels of noise caused by the switching nature of the computer's power supply, linear voltage regulators were implemented in the module's power paths. In addition to an LC input filter, multi-stage linear regulation was used to minimise supply noise. As a result, the current drawn from the 5 V USB source matches the total current consumed by the counter at various voltages from 1 V to 3.3 V. This additional power loss reduces efficiency but is necessary to maintain measurement precision.

## 4. Test results

The designed interpolated time counter was tested using a custom-built prototype *printed circuit board* (PCB), shown in Fig. 6(a). The board features four signal inputs with an input impedance of 50 Ω. Three of these inputs are dedicated to recording input events and support an input voltage range of ±5 V, with an adjustable threshold voltage in 1 mV steps. Each of these inputs can also be optionally configured to accept an external trigger signal. The counter includes an onboard *temperature compensated crystal oscillator* (TCXO) that provides a 10 MHz

reference clock with a stability of $2 \times 10^{-8}$. Alternatively, an external high-stability clock source (*e.g.*, an atomic clock with a maximum signal level of 1 $V_{rms}$) can be connected via the fourth SMA input. One of these clock sources is used as the reference clock for the onboard frequency synthesiser, which generates the 300 MHz main clock for the integrated time counter. The board is powered and controlled via a USB 3.0 interface, which also supports the USB Power Delivery protocol.

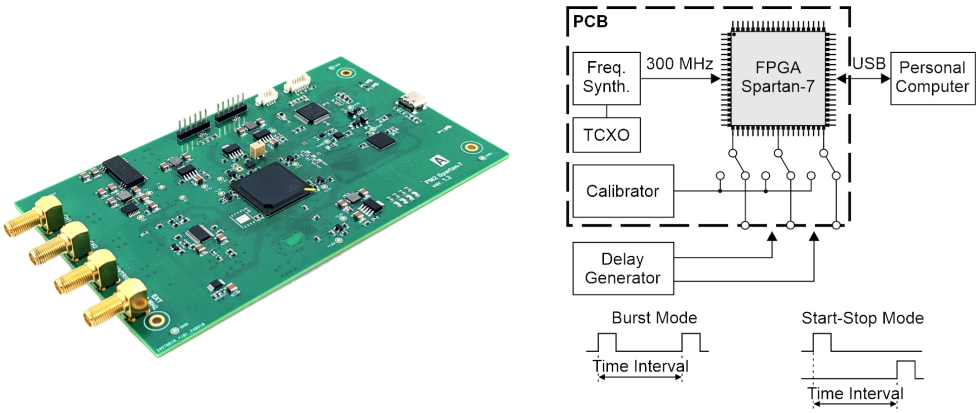



Fig. 6. (a) Prototype PCB with the integrated time interval counter and (b) the test setup.

### *4.1. Test setup*

Figure 6(b) presents the test setup used to characterise the parameters of the developed time interval counter. The on-board calibrator generates a square-wave signal, which, for the purposes of calibration procedures (SCDT), is connected to the integrated time counter instead of the measurement signals. The test time intervals are generated with the use of the Model 745 digital delay generator from Berkeley Nucleonics Corporation [33].

The parameters of the counter were evaluated in two modes: burst and start-stop. In the burst mode, the time intervals are defined by the rising edges of two consecutive pulses of a square signal applied to a single counter input. Thus, the measurement is performed on one selected channel. In the start-stop mode, the start pulse is applied to one counter input while the stop pulse is attached to another, resulting in an inter-channel measurement. The counter configuration and data transfer are managed via a USB interface. All tests were conducted under laboratory conditions, at an ambient temperature of approximately 21°C.

### *4.2. Resolution and nonlinearity*

On start-up or on demand, the code processor initiates a calibration procedure based on the SCDT. A square-wave signal from the calibrator – uncorrelated with the main clock – is used as a source of random time intervals for the TDC. The counter collects 2 million random samples, based on which the probability of occurrence of various digital codes in the TDC is calculated.

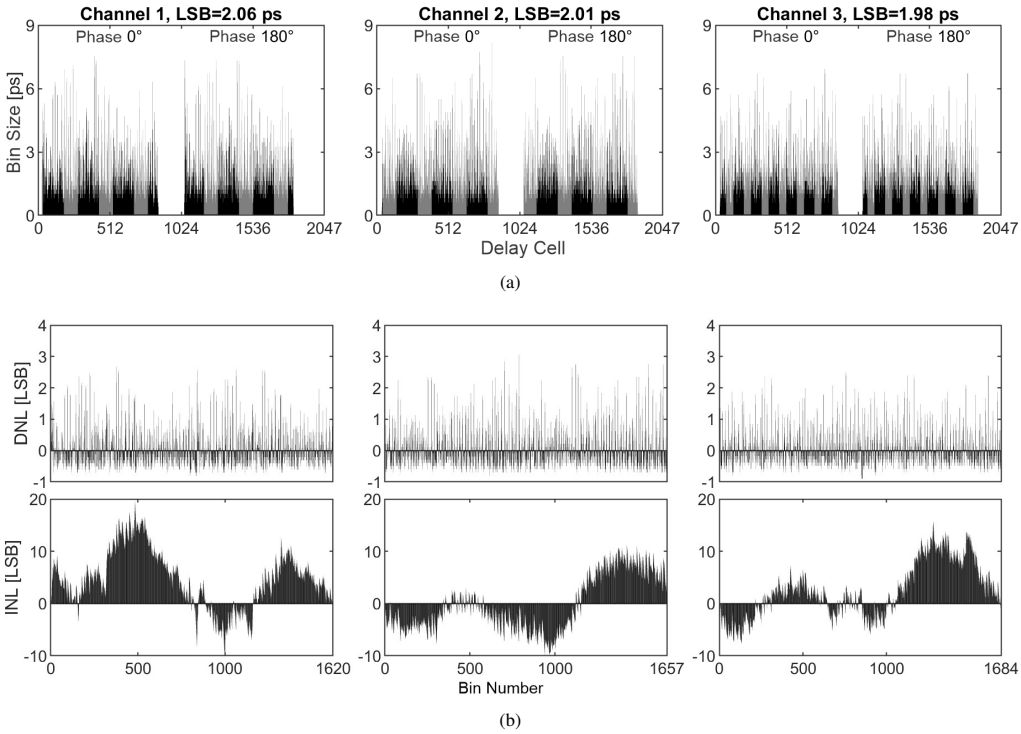
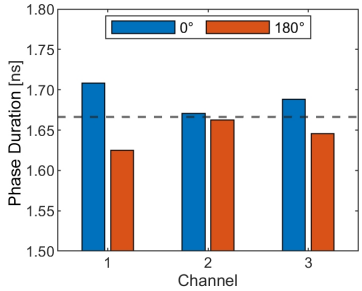



Fig. 7. (a) Results of the SCDT with bin sizes and (b) nonlinearity plots (DNL and INL).

By multiplying the obtained probabilities by the TDC measurement range, the actual bin sizes are determined. The results for all three measurement channels are presented in Fig. 7(a). These characteristics reveal a split between the results obtained from the SIS during the first (0°) and second (180°) phases of the main clock signal. In every case, the resolution, defined as the size of LSB, is approximately 2 ps (only nonzero bins are considered). However, there are distinct differences between individual delay cells. These differences are illustrated in the *differential nonlinearity* (DNL) and *integral nonlinearity* (INL) plots shown in Fig. 7(b), where digital codes that never occur have been omitted and only nonzero bins are considered. Taking into account both the quantisation error and the nonlinearities, it can be estimated that the designed two-stage TDC behaves as an ideal TDC (DNL = 0 LSB) with an equivalent resolution of about 3.0–3.3 ps [7]. Due to the code processor, which computes the measurement result based on the actual transfer characteristics, the influence of nonlinearities on the precision is significantly reduced.

From the SCDT results, the phase uniformity can also be determined. Fig. 8(a) shows the differences between the durations of the 0° and 180° phases. The phase of the clock signal is selected by a multiplexer in the programmable logic block, where the clock signal is routed to the FF through either a buffer or an inverter. The difference in durations of these phases is mainly attributed to the disparate propagation times of these two elements, along with process variations and clock skew. In the end, the two phases differ by up to a few percent (up to 5%, equivalent to 83.6 ps), which increases the required measurement range in the SIS. A summary of the resolution and nonlinearity of the counter is provided in Fig. 8(b).




(a)

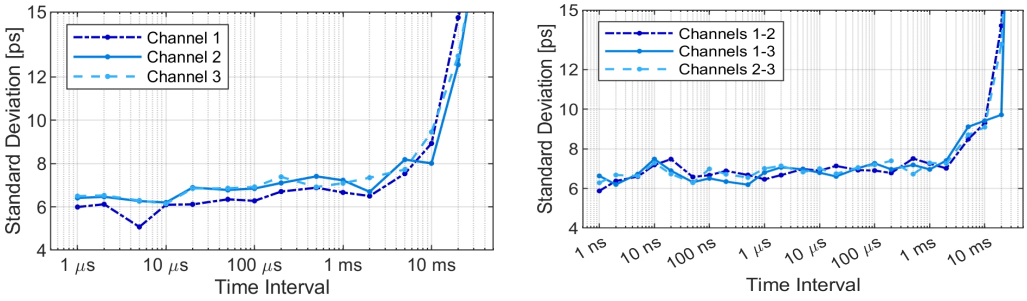
| | Channel 1 | Channel 2 | Channel 3 |
|---|---|---|---|
| **LSB [ps]** | 2.06 | 2.01 | 1.98 |
| **$LSB_{eqv}$ [ps]** | 3.25 | 3.27 | 2.96 |
| **Phase difference [%]** | 5.02 | 0.50 | 2.55 |
| **DNL [LSB]** | [–0.80; 2.66] | [–0.90; 3.05] | [–0.90; 2.49] |
| ***Std*(DNL) [LSB]** | 0.61 | 0.64 | 0.56 |
| **INL [LSB]** | [–10.28; 19.42] | [–9.80; 11.07] | [–7.67; 15.63] |

(b)

Fig. 8. (a) Phase uniformity and (b) a summary of the TDC nonlinearity.

### *4.3. Standard uncertainty*

The precision of the integrated time interval counter was evaluated by recording an arbitrarily selected set of 2000 timestamps, either in a single channel (burst mode) or across two channels (start-stop mode). This yielded 1000 time interval measurements, swept from 1 ns to 50 ms. In the burst mode, the lower bound of the measurement range (1 µs) was limited by the capabilities of the delay generator. Precision was calculated as the standard deviation of the 1000 measured time intervals between the start and stop pulses (Fig. 9).




(a) (b)

Fig. 9. Integrated time interval counter precision (a) in the burst mode, (b) in the start-stop mode.

In both operating modes and across various channel configurations, the counter maintained a precision better than 8 ps within a measurement range of up to 2 ms. Considering that each time interval is determined from two timestamps, the estimated single event registration precision is better than 5.65 ps (8 ps/$\sqrt{2}$), which proves the high performance obtained in a low-cost FPGA chip.

## 5. Conclusions

This work demonstrates that precise, multi-channel time interval measurements can be achieved using compact and inexpensive FPGA devices. The proposed time counter, implemented in a Spartan-7 (AMD/Xilinx) programmable device, successfully integrates a timestamping method with a two-stage interpolation based on an enhanced TDC architecture. The use of multi-edge

coding in four independent TDLs and an efficient encoder provides high resolution while minimising resource utilisation. The developed counter, conveniently controlled and powered via a single USB port, achieves an equivalent resolution of approximately 3 ps and a single event registration precision better than 5.65 ps, with a measurement range extending up to one hour. These high metrological parameters are achieved with a relatively low power consumption of about 0.5 W. The presented results confirm the practicality of implementing advanced time measurement solutions in cost-sensitive and space-constrained applications, such as portable low-power instruments that can effectively compete with expensive desktop devices in many areas, *e.g.*, clock monitoring, time and frequency distribution, as well as in various physical and technical experiments.

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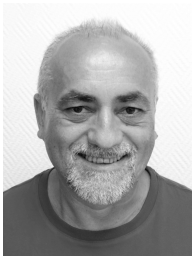

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